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PRELIMINARY TESTS OF DIGITAL PULSE SHAPE ACQUISITION FROM CHIMERA CsI(Tl) SCINTILLATORS

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Abstract

A sampling digital to analog converter (12-bit, 100 MS/s) has been used to perform a digital pulse shape acquisition of the signals coming from a typical CHIMERA 6x6x12 cm^3 CsI(Tl) scintillator coupled to a standard CHIMERA electronic chain, up to the amplifier. The preliminary results obtained with Tandem beams are presented.

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1 INTRODUCTION

CsI(Tl) scintillators are widely used to perform Light Charged Product (LCP) identification, as they emit light pulses whose shape varies with the type of incident radiation. As well known, the decay of the light emitted by the CsI(Tl) is parameterized by the sum of two main components (exponential functions):

$$L(t) = L_F\ e^{-\left(\frac{t}{\tau_F}\right)} + L_S\ e^{-\left(\frac{t}{\tau_S}\right)}, \qquad (1)$$

where τ_F and τ_S denote the decay constants of the fast and slow components of the light pulse, respectively.

Discrimination among particles is then possible because the ratio of Fast and Slow amplitudes (L_F/L_S) varies with the particle type and the ionization density of the particle. Consequently the ratio of the pulse heights at two different times, t_1 and t_2, depends on M, Z, and E. Thus the integration of a portion of the tail of the amplifier output and the plot of this value (Slow-component) versus a value proportional to peak value (Fast-value) allows to identify in mass and charge light charged particles (LCP).

In order to improve the on-beam and on-line LCP identification for the CsI(Tl) crystal, we have performed a real-time digital pulse-shape analysis of the signals coming from a CsI(Tl) scintillator of a CHIMERA [1] detection cell, by using a part of the standard electronic chain used in CHIMERA for measuring the Slow component, and a sampling analog to digital converter instead of the charge analog to digital converter. In the present report the results obtained on-beam and on-line are presented.

2 EXPERIMENTAL SET-UP

In view of new perspectives in nucleus-nucleus Isospin physics by using both stable and exotic beams and the consequent 4π AZ multidetector projects [2], we have implemented an ad hoc system to digitally compute Fast and Slow components for a typical CHIMERA scintillator. We have carried out some tests using sampling digital to analog converters (sampling ADC) to perform a real-time digital pulse-shape analysis of the signals coming from a standard CsI(Tl) scintillator of CHIMERA, coupled to a photodiode. This work has been motivated by both the increasing employment of digital pulse shape analysis in γ-spectroscopy and our previous experience in on-line digital signal processing [3,4]. To date, only few results obtained off-line with radioactive sources and small crystals (1 cm^3) have been reported on digital processing of CsI(Tl) signals [5]. The use of fast sampling ADCs presents some advantages with respect to the analog treatment, as listed in the following:

possibility to implement optimal filters which are hardly carried out with analog techniques;

insensitivity to pick-up noise, as soon as the signal is digitized;

flexibility and possibility to periodically recalibrate the system with S/W procedures;

reduction of the complexity of the electronics in 4π AZ multidetectors;

possibility to implement on-line computation of complex and very effective algorithms directly on the shape of collected pulses.

2.1 Analog electronic chain

For CHIMERA, the classical two gate method [6] based on the charge comparison between Fast and Slow components is applied to collect Fast and Slow signals. In Fig. 1 the typical electronic chain for a CHIMERA CsI(Tl) scintillator is shown. In the following we call this kind of electronic chain *analog chain*. The crystal (6x6x12 cm^3 wide) is coupled to a Hamamatsu photodiode (PD) (18mm x 18mm x 300_m), connected to a charge preamplifier (PA), and to a 16-channel SILENA 761F spectroscopy amplifier (A) [7] (2_s shaping time). The two output pulses, one shaped for collecting the Slow, the other stretched at maximum value to give the Fast, are simultaneously converted 8 μs after the starting point by two 9U QDCs [8] (Fig.1). The gate generation method is described in [9], where the analog particle identification in the CsI(Tl) crystals used for CHIMERA 4π detector is also reported.

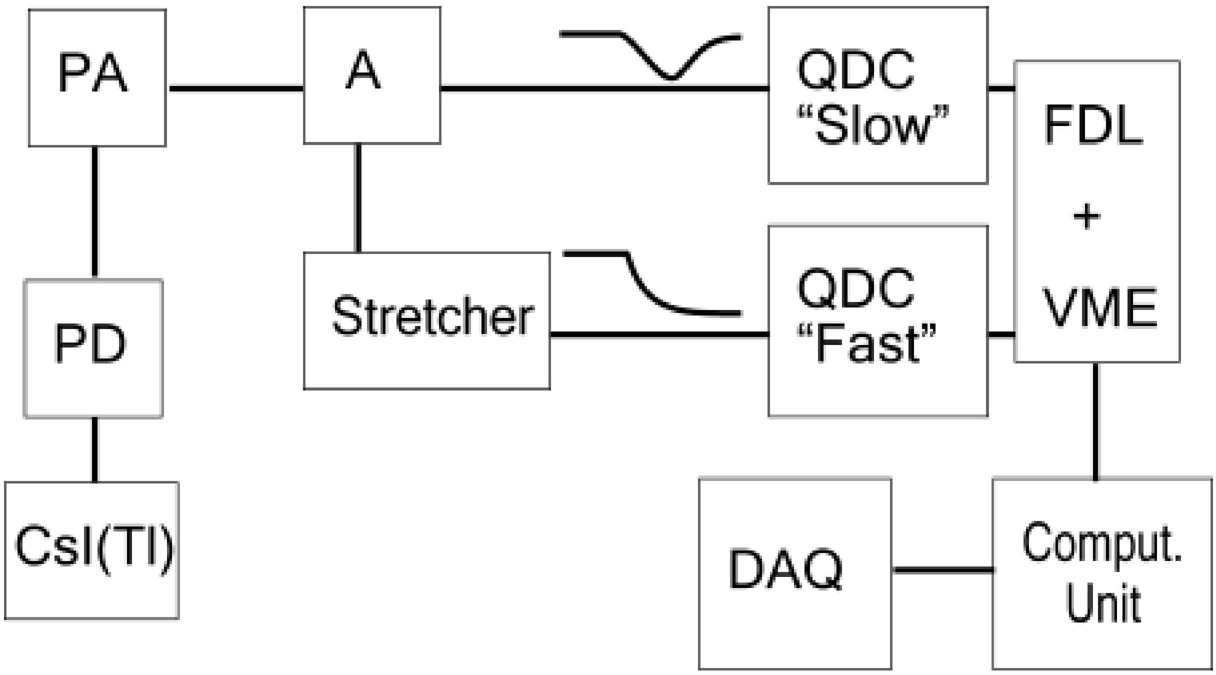

FIG. 1: Standard analog chain for Fast and Slow acquisition.

2.2 Digital electronic chain

Let us call *digital chain* the electronic chain we used to perform the tests we describe here (Fig.2). The modules up to the amplifier were unchanged. The shaped output from the amplifier was fed directly into the sampling ADC input.

The trigger for the acquisition was generated by an ORTEC constant fraction discriminator using the tune signal delivered by the SILENA amplifier.

The sampling ADC used is a SIS3300 [10], 8 channels 6U VME digitizer/transient recorder with a sampling rate of up to 105 MHz for the individual channel and 12-bit resolution. The board multievent and dual memory bank functionalities make the card a good choice for our applications. It allows for 6 different sampling frequencies: from 100 MS/s down to 3.125 MS/s. It is also able to use an external sampling clock. Each channel has two dedicated memory banks, both 128 KS deep, that can be used in a "ping-pong" fashion, that is new data can be stored on one of the two banks while previously sampled data are being retrieved from the other one. Those memory banks can be segmented in up to 1024 (equal) pages, corresponding to pages from 128 KS down to128 S long, in order to store many events, one for each page. Two dedicated LEMO trigger inputs are placed on the front panel: a start trigger input (to be used with ADC set in START mode) and a stop trigger input (ADC STOP mode). In START mode the ADC starts sampling on trigger signal and stops automatically at the end of the page. In STOP mode it samples continuously, using the same page to store data, and so overwriting new data upon old ones. This feature is called WRAP AROUND, and is necessary when using ADC stop mode. When the trigger occurs, the ADC writes the address of the sample after the last (in time order) one in a bank of registers called EVENT DIRECTORY BANK, and starts writing on the next page. When working in STOP mode (with WRAP AROUND) the events need to be reconstructed in time order. The first sample to be taken(i.e. the oldest in the page) is the one having its address recorded in the EVENT DIRECTORY BANK. Then the following samples are taken, to the end of the page. The next one to be considered is the first of the page, and then all the following, to the last one recorded.

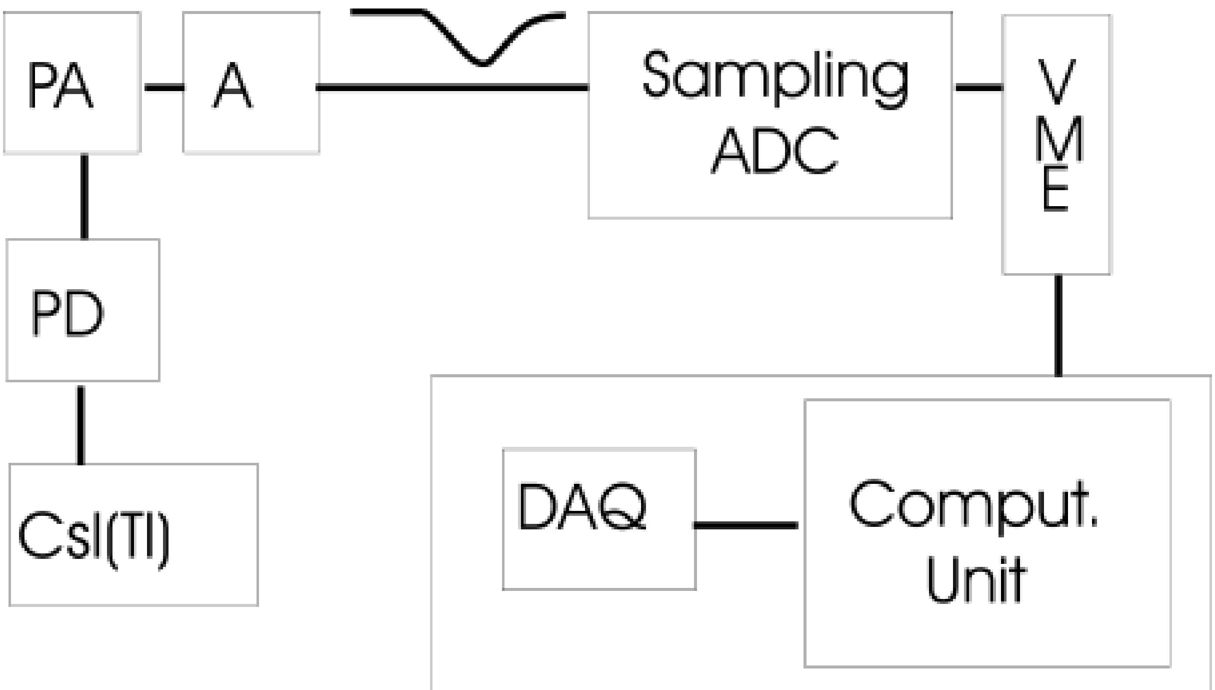

FIG. 2: Digital chain used for Fast and Slow acquisition.

A delay on the trigger, both in start and in stop mode, can also be programmed in the ADC, such that the sampling starts or ends, respectively, after a user defined number of sampling clock pulses. The ADC is able to send a VME interrupt whether a page is full (end of event mode) or a whole memory bank is full (end of last event mode). Together with the sampling

ADC, in the VME crate its manager CPU is placed: the VP7 [11] embedded CPU VME module. VP7 is a 6U all-in-one VME-bus CPU based on Pentium III processor (700 MHz). A host PC was connected to VP7 via Ethernet 100 Mb/s for presenting the results and for recording them on tape.

2.3 System management

VP7 was used as manager CPU for the sampling ADC. Via VME bus it collected the digital samples and stored them in a buffer, at the same time reconstructing the Fast and Slow components, by means of the charge comparison method. The main thread running on VP7 starts presenting the user a dialog box through which to set program options: about sampling ADC configuration, sampled data storing, etc. Then it opens a Master access window on VME and configures the sampling ADC. The system is then ready to start acquisition. The amplifier output signal was 20 μs long (1 signal = 1 event = 1 page). We set a length of 2 KS for the pages, that is 64 events per bank, when sampling at 100 MS/s (one sample every 10 ns) and a length of 512 samples per page, corresponding to 256 events per bank, when sampling at 25 MS/s (one sample every 40 ns). The trigger occurred after the signal began, but before its end, so we configured sampling ADC in STOP MODE (with WRAP AROUND) and STOP DELAY. Finally we used "END OF LAST EVENT" interrupt generation mode. On VP7 the acquisition thread waits for ADC interrupts. When one occurs the thread activates the other bank and starts reading the full bank. Then the events are reconstructed as already explained, and stored in binary files. We established a straight format for those files: each bank starts with one datum specifying bank segmentation, then all the samples are stored, and a termination value (0xFFFF) is written at the end of each page/event. The number of banks to be stored in each file can be set in the (initial) configuration dialog box. So a number of files can be created for each sampling session, of a fixed length. From reconstructed events, the Fast and Slow components were also computed, using the charge comparison method, and stored in other files. Fast-Slow matrices could thus be visualized on the Ethernet connected PC, allowing for partial results to be checked, while the experiment was running. While sampling proceeds, on VP7 the main thread waits for the user to stop acquisition: then stops the ADC and closes the VME Master window.

In Fig.3 the block diagram of the code running on VP7 and handling the acquisition, is shown. It is written in Visual C++ and runs under Windows NT 4.0 O.S..

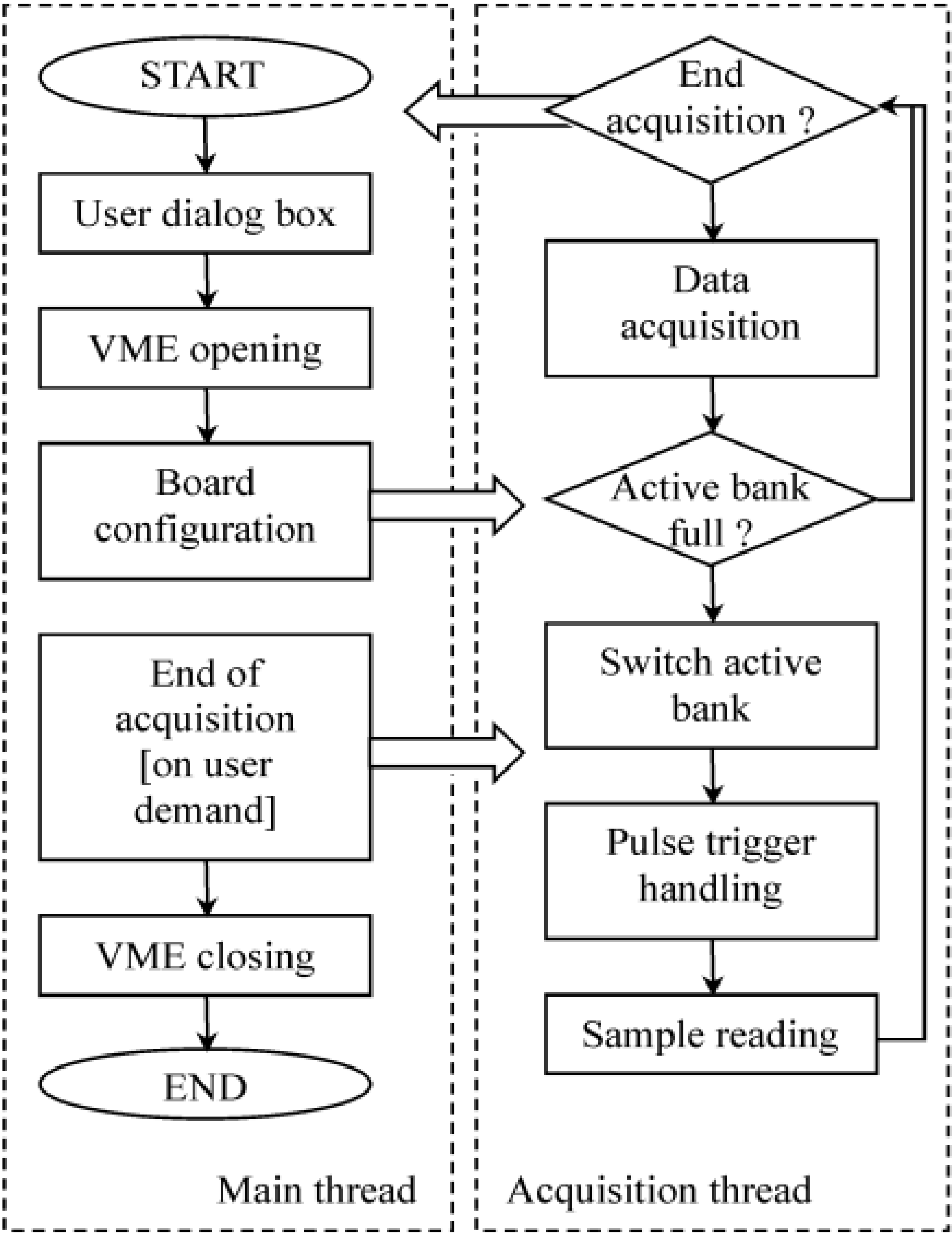

FIG. 3: Acquisition code block diagram.

In Fig. 4 the user dialog box of the program is shown. It allows to set the typical working functionalities of the ADC and the parameters used for the on-line computing of the Fast-Slow components.

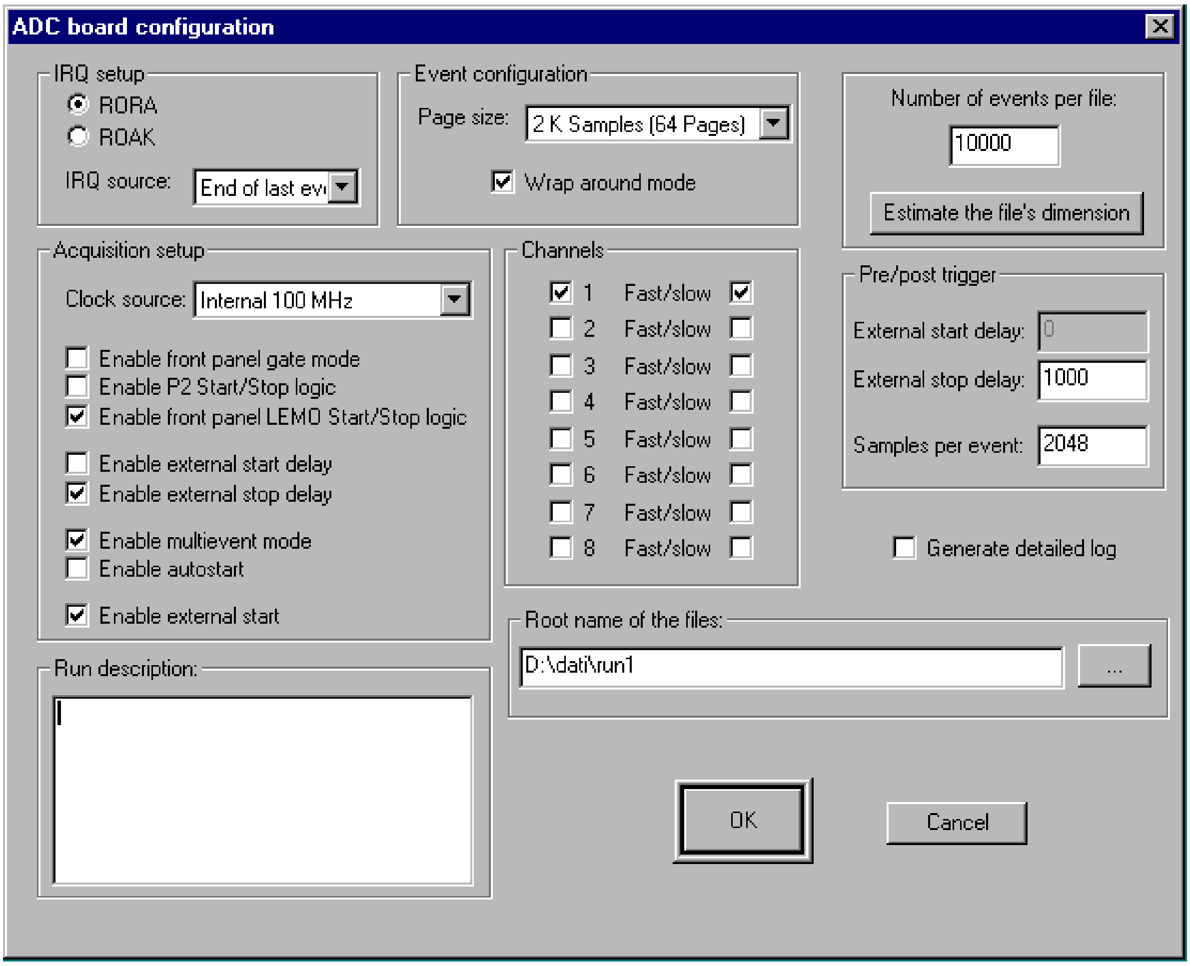

FIG. 4: User dialog box of the program.

3 EXPERIMENTAL RESULTS

In the present tests, the shape of the amplifier output was up to 20 µs long (Fig.5). We worked at two different acquisition frequency: 100 and 25 MS/s. For every event, the sampling ADC recorded a signal-form with 2048 (512) consecutive digital samples, collected at 100 MS/s (25 MS/s), i.e. at 10 (40) ns time intervals. In the two cases, no appreciable differences were seen in the pulse shape reconstruction.

The reached acquisition rate was of ~ 600 Hz (for 25 MS/s), fully compatible with CHIMERA acquisition rate.

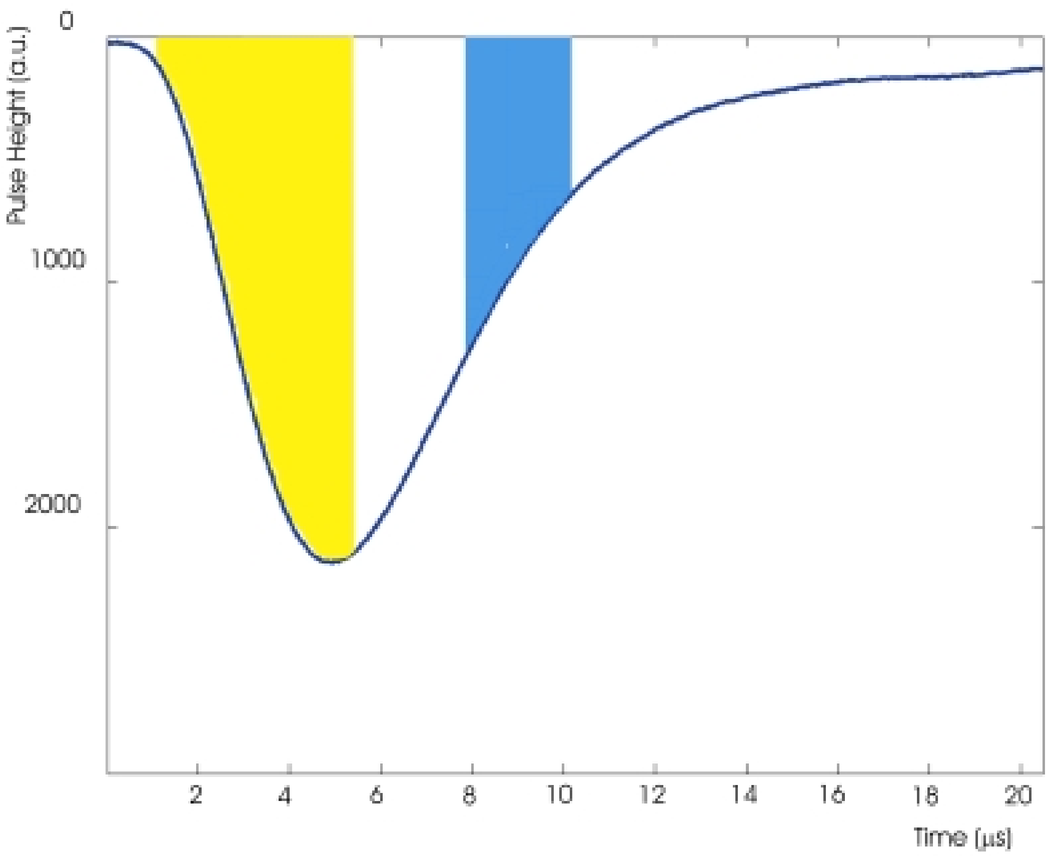

FIG. 5: Typical amplifier output signal, digitally collected, with enlightened the Fast and Slow components

A typical 6x6x12 cm^3 CsI(Tl) scintillator placed in a telescope behind silicon detector in the 2000 scattering chamber of LNS gives the residual energy of detected heavy ions and, in case of light charged particles, allows for identification of their charge and mass.
Beams of ^{7}Li delivered by the LNS tandem at 52.5 MeV were used to bombard a polypropylene (deuterium enriched) target. The reaction products were detected at _=8° in the laboratory system. In Fig.5 a CsI(Tl) pulse shape after a standard CHIMERA amplifier together with the FAST and SLOW integration zones is shown.
In Fig.6 the Fast vs. Slow matrix for this reaction is reported. It has to be noted that ^{7}Li are not detected because of the presence of the Silicon detector in front of the CsI(Tl).
A ^{16}O beam at 102 MeV incident energy bombarded a selfsupporting ^{12}C target 100_g/cm^2 thick. A standard CHIMERA CsI(Tl) scintillator was mounted at _$_{lab}$=10°, with no silicon detector in front. Fig.7 shows typical features of the identification.
Present results proved competitive or at least comparable with respect to those obtained with the standard analog treatment, allowing a considerable saving in electronics modules. Moreover they showed the power of digital shape acquisition in achieving good light particle identification with large dynamical range.

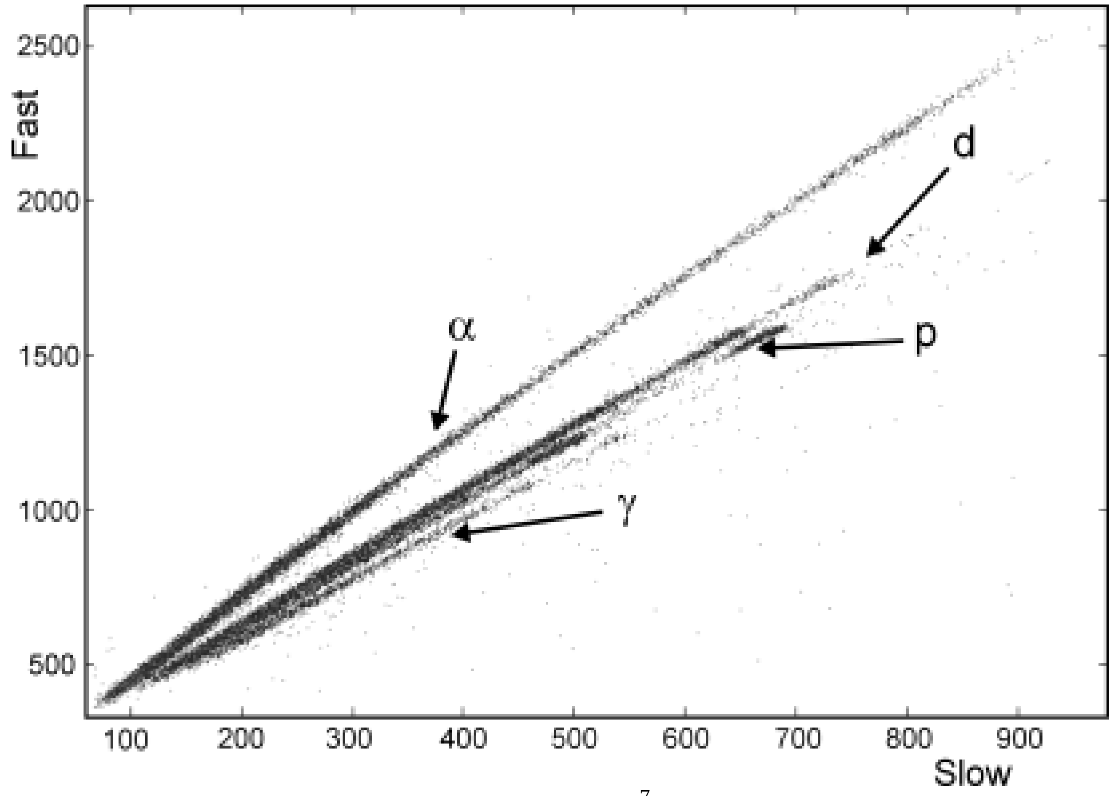

FIG. 6: Results obtained with ^{7}Li incident beam.

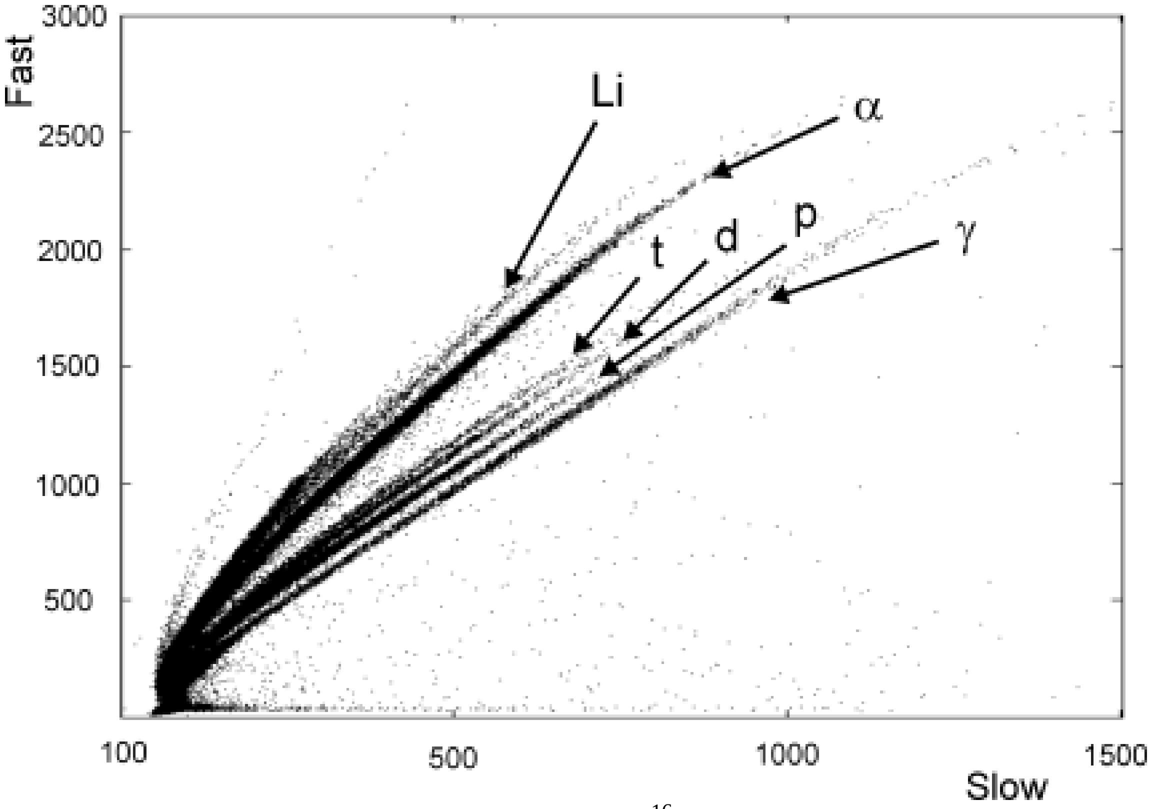

FIG. 7: Results obtained with ^{16}O incident beam.

4 ACKNOWLEDGMENTS

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