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Data Acquisition System for E-835 Silicon Detector

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Abstract

In this paper we describe the DAQ system for the Silicon Pad Detector used in experiment E-835 at Fermilab.

It is composed of three different electronic boards that perform detector read-out, zero suppression and store data in a VME memory segment.

The system is based on high performance VLSI custom components for data encoding and zero suppression to achieve the maximum reliability and performance. Furthermore, all logic functions have been implemented using FPGAs to handle the second level trigger.

The whole system has been fully tested at CERN in november 1995, installed at Fermilab in september 1996 and is now operational.

1 Introduction

The goal of the experiment E-835 is to complete the study of charmonium spectrum by forming all resonant states in proton-antiproton annihilation, using an internal jet target installed within the Antiproton Accumulator at Fermilab (see [1] [2] [3] [4] for details). The experimental apparatus is a non-magnetic spectrometer composed mainly by a very compact inner tracking system, a threshold Cerenkov counter and an electromagnetic lead glass calorimeter.

In 1997 data taking run one of the main challenges of experiment E-835 is the detection of the η_c resonance in the $\Phi\Phi \rightarrow 4K$ channel, mainly using the informations coming from the tracking detectors.

This tracking system is composed, among other elements, of a Silicon Pad Detector[5] [6], whose DAQ electronics has been designed and built by our group together with the detector itself. This DAQ system is the subject of this paper.

This design has been dictated by several constraints and requirements:

- the data throughput: E-835 instantaneous luminosity is $3.0 \cdot 10^{31} \text{ cm}^{-2}\text{s}^{-1}$, so the trigger rate can be as high as 10 kHz . In this case the data flow from the detector is around 1 Mbyte/s in normal conditions.
- the compatibility with the other part of the DAQ system: E-835 DAQ is based on a system developed at Fermilab which uses a special CAMAC controller [7] (DYC) that reads out all ADCs and TDCs using the fast ECL port and stores all the data in a buffer. This buffer is read asynchronously by a VME master through an interface. The readout system that is described in this paper behaves exactly like a DYC, so it is fully compatible with the existing system, allowing the master to read the ROC just as it were a DYC.
- the availability of the two main components of the system: ICAR16¹ chip as front-end amplifier and of the FEROS² chip for encoding and zero suppression.

A simple block diagram of the whole system is shown in figure 1: it is composed of: 8 Slab Coding Boards (SCB), which perform data read out, zero suppression and coding; the Feros Bus Interface (FBI), which handles the communication protocol between the SCBs and the system Master, the Read Out and Control board (ROC), a the VME slave which controls the whole system.

¹ ICAR16 is supplied by Smart Silicon System, Avenue de Chailly, 23 CH 1012 Lausanne Switzerland.

² The FEROS is a gate array developed at CERN by G. Schuler for the WA92 experiment. In this project we do not use the internal circuit that implements a distributed adder.

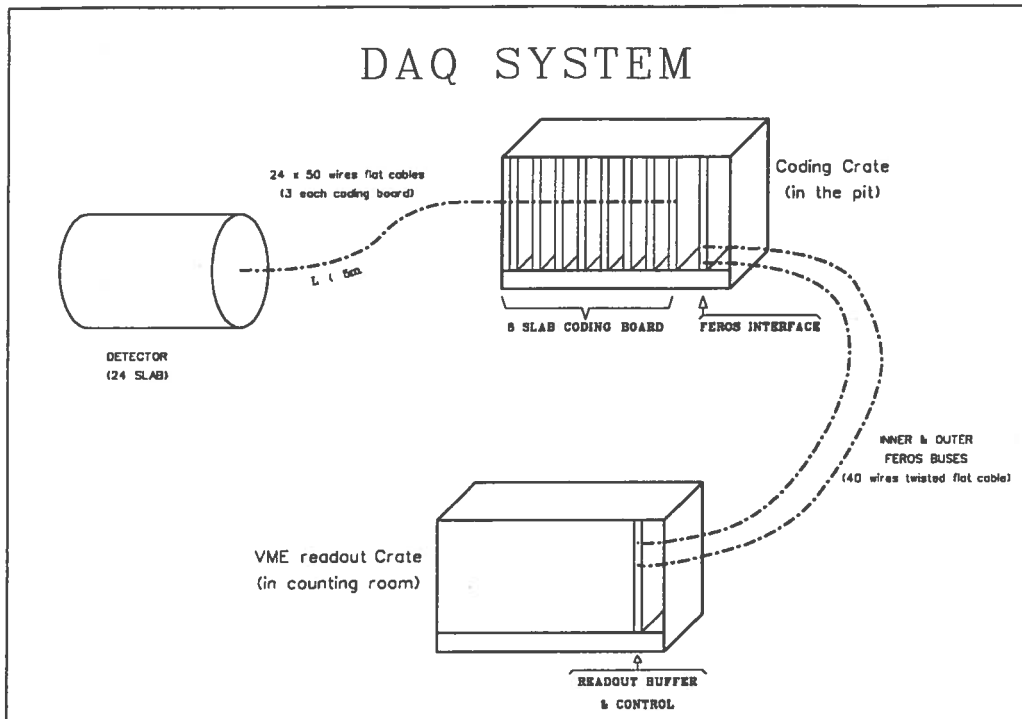


Fig. 1. Block diagram for the Silicon Pad Detector DAQ system. The detector, the 8 Slab Coding Board, the Feros Bus Interface and Read Out and Control module are schematically shown. Data are read and encoded by each SCB and then transferred to the ROC via FBI and stored on a VME-readable FIFO memory.

The signals coming out of the detector (see cited references for details) arrive at the SCBs via 24 flat cables, each carrying the information of 192 channels as 12 multiplexed ECL lines with 16 channels each. The 8 SCBs are housed in a VME crate whose distance from the detector must be within 5 m. Then all coded data are sent to the Read Out and Control Module (ROC) through the Feros Bus Interface (FBI) and stored on a VME readable memory segment.

This paper is structured as follows: section 2,3 and 4 give a brief description of the system; for further details see [8],[6]. In section 5 performances and test results are discussed.

2 The Slab Coding Board

Each SCB performs read out and coding of non-zero data coming from 3 different detector modules ($192 \times 3 = 576$ channels). SCB design is based on FEROS chip, that has been developed to control and read out the front-end amplifier ICAR16 used for the detector. Each FEROS reads 96 channels, performs zero suppression and coding. All FEROS of the 8 SCBs are connected in

2 different daisy chains, corresponding to 2 independent layers of the detector, referred as INNER and OUTER. The chaining is initiated by the local control board (the FBI), which receives the end of the chain and detects the end of the data stream for both INNER and OUTER buses.

A complete description of this board can be found in [8].

3 The Feros Bus Interface

It performs the following functions:

- (i) For each trigger signal (either hardware or software) it generates the control signals to be sent to the ICAR16 on the SLABs (via the SCBs) and to the FEROS chips on the SCBs.
- (ii) It manages two external asynchronous buses (called FEROS buses), one for each detector layer. These buses carry the silicon pads data to be read by ROC and the commands issued by the master controller.
- (iii) It executes the commands issued by the read out controller: software reset, software trigger, write DAC setting, set DACs, reset DACs settings.
- (iv) It handles the SLABs discriminators threshold loading.

3.1 Generation of control signals

This circuitry is triggered by a NIM signal (STROBE) or by a software trigger issued by the ROC.

Figure 2 shows the control signals, whose meaning is the following:

- TH_CS: it is the hold signal for the charge preamplifier ICAR16. It is generated with minimum delay from the STROBE.
- CK_LT: After 100 nsec from the leading edge of TH_CS 17 clock pulses with 50% duty cycle are generated with 200 nsec period (5 MHz frequency). This signal has three functions: on the leading edge it extracts the analog data from the preamplifier; on the trailing edge it latches the comparators outputs; with the next leading edge the digital data are loaded into FEROS.
This pipelined system is the most efficient to handle the data transfer between the detector and the SCBs. The limit of 5 MHz frequency is imposed by the propagation delay on the flat cable. We need about 3.5 μ sec (200 nsec \times 17) to read the whole detector.
- XLOAD: Is the signal used to indicate the end of loading data into the FEROS.
- XCLEAR: Is generated at the beginning of the sequence and it is the RESET to the FEROS.

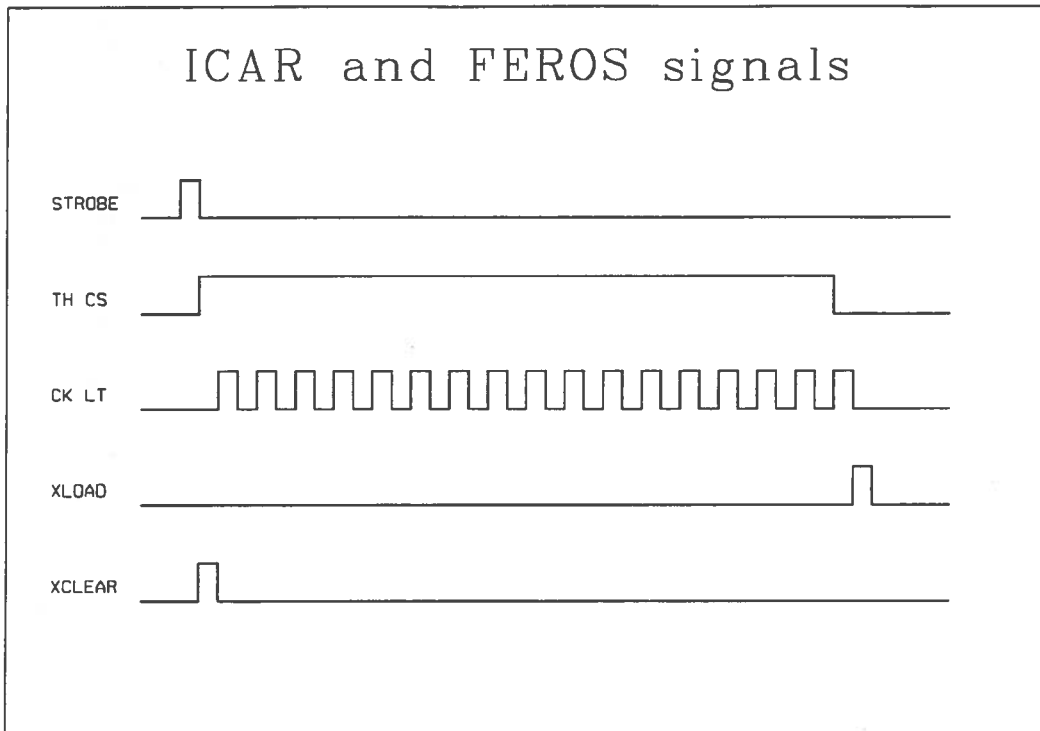


Fig. 2. The ICAR16 and FEROS Control Signals

At the end of the generation of this control signals sequence it is possible to read the coded data from FEROS. This is carried out generating a read request on the external asynchronous buses from the ROC.

3.2 The Feros Bus

We need an very good transmission system to transfer the data in the control room because the long distance between FBI and ROC that could be up to 30 meters. To handle the communication between the FBI (in the pit, near the detector) and the ROC (in counting room) we implemented an asynchronous, point to point, master-slave protocol.

It is always the master (ROC) that can start a bus operation; the slave (FBI) answers to the issued command with a status condition and the acknowledge.

We implemented two equivalent buses to handle data coming from the two detector layer in an independent way. In particular only the INNER bus is used to issue commands to the FBI, while the OUTER one is used only to read data. A more detailed description of these buses can be found in [8]. The readout speed of this bus is limited by FEROS to 10 Mbyte/s.

Two commands are related to DAC settings. All 288 thresholds are stored in a FIFO and then distributed to SCBs which deliver them to the detector. The whole loading sequence needs about 5 *ms*.

4 The Readout and Control Unit (ROC)

The ROC is a VME module specifically designed for the management of the entire data acquisition system of the Silicon Pad Detector.

It has an additional local control port to connect a personal computer via a parallel interface to its internal devices: with this facility, it is possible to debug easily the system also when all the DAQ programs are up and running.

To have the maximum flexibility and compactness the board was designed using some FPGA as main logic components. We used XILINX components in order to have the possibility to change the configuration of the board very quickly and late in the development process: this was a mandatory constraint because at the beginning of the project the collaboration ask us to foresee a possible 2nd level trigger signal which was non used in the experiment. To have the possibility to accept or reject this additional trigger signal the board is equipped with two levels of temporary memory buffer³ In the actual configuration the board controller ignores this signal and simply copy the data between the two buffers. If this signal has to be used the controller can be easily reconfigured to make the copy process only if the event data are accepted by the 2nd level trigger logic.

In figure 3 a detailed block diagram of the ROC is shown.

4.1 VME specifications

The ROC is a VME slave device, with no master capability.

Only extended (32 bit) addressing is supported. Standard and short addressing (24 and 16 bit) are not supported. The board will respond to privileged and non privileged data and program address modifier codes (AM codes: 09, 0A, 0B, 0D, 0E, 0F⁴).

³ These buffers are implemented using FIFO components.

⁴ In the following description all numbers are represented using hexadecimal notation unless otherwise noted.

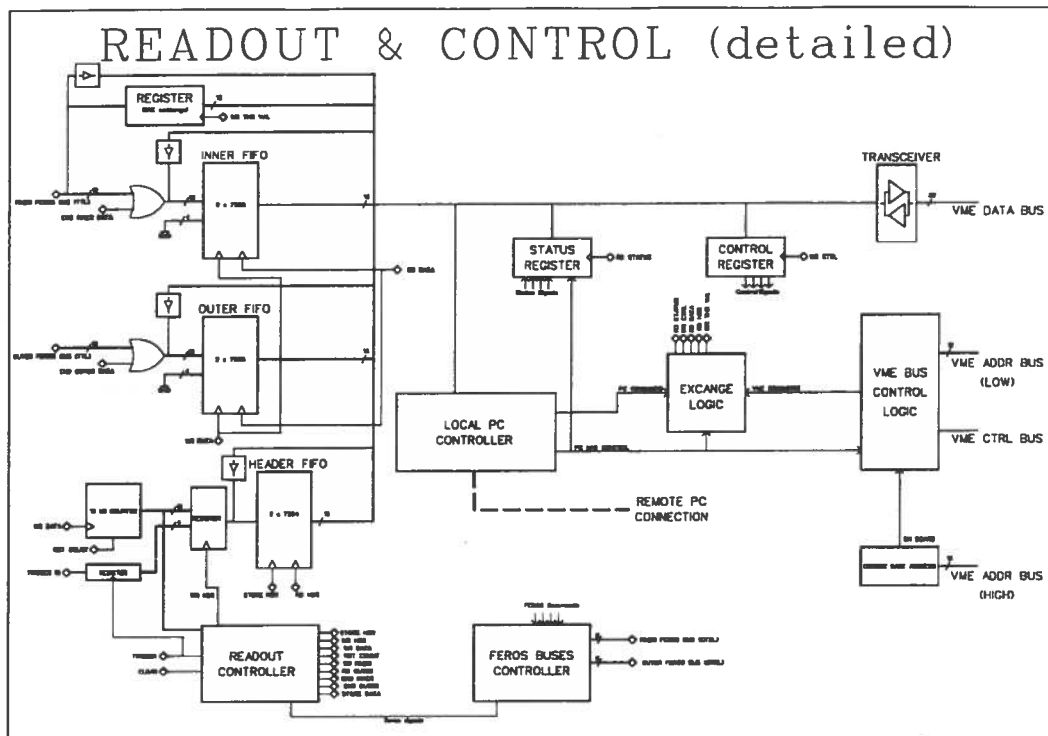


Fig. 3. Detailed ROC Block Diagram

Only longword (32 bit) aligned data transfers are supported. Unaligned data transfers, word transfers and byte transfers (16 and 8 bit) are not supported.

Single VME cycles and pipelined single VME cycles are supported, block transfers are supported as well, during the readout of data buffer.

No interrupt capability is provided: the master must poll the status register to see if there are data to read.

4.2 ROC memory map

The lower 32 Kbytes (8 Klongwords, from 0000 up to 7FFC) provide access to the data buffer, which is organised in a FIFO fashion. A range of addresses is provided so that the VME master can read data with a single block transfer cycle.

The first address (0000) contains the data header, whose 12 less significant bits contain the number of words of each event and 4 additional bits store the trigger ID coming from the ESN module [10]⁵.

⁵ It is the module used to generate the trigger identification number in E-835 DAQ system.

The following addresses (0004, 0008, . . . , 7FFC) contain data coming from the detector.

At address 8000, 8004 and 8008 there are the DAC register, the Status Register and the Control Register.

All commands are issued to ROC by writing on the Control Register a proper bit while ROC response and status is retrieved by polling the Status Register.

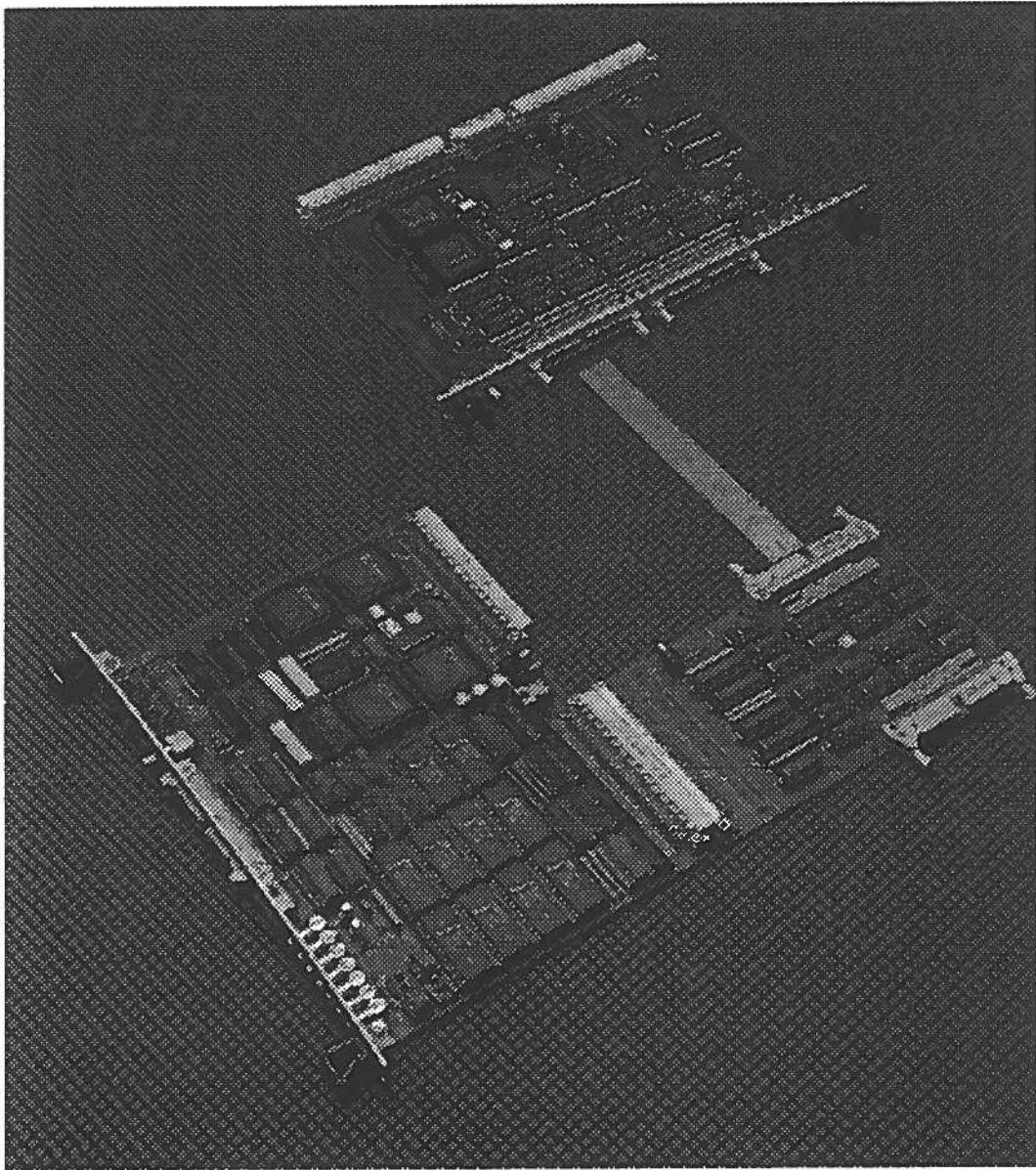


Fig. 4. This picture shows the two main boards of the system: ROC (bottom left) and the FBI (top right). The small printed board (bottom right) is the receiver and TTL/422 converter of the FEROS bus signals.

5 Performances

The VME system we used for testing was based on a FIC8234 controller: a 68040 cpu board, supplied by CES⁶, equipped with 8 Mbytes of RAM, an hard disk, a floppy disk and an ethernet controller. The Microware OS9 operating system was installed on this unit.

This system has worked to test the detector on a test beam at CERN⁷ in fall 1995. See [5] for test results. Now, in the final installation, the controller is a Motorola MVME167 with the VxWorks operating system⁸.

The system can read each couple of silicon pad data from FBI every 300 nsec. In this configuration we are able to read the whole detector ($96 \times 24 = 2304$ words) in less than $700 \mu\text{sec}$ ⁹.

With an event size of about 50 words per event coming from the detector, the averaged read out time is about $20 \mu\text{s}$ per event. At a trigger rate of 3 KHz the dead time is less than 10 %.

Acknowledgement

We would mention here the persons that helped us in this job.

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Giancarlo Barisone, Marco Negri and Pasquale Poggi (INFN Genova) have worked principally at the detector assembly, mechanics and silicon crystals characterization, but they also did a precious job in the test beam set up at CERN.

We would also thank Prof. A. Santroni and dott. M. Macri⁰ for their advices and encouragement.

⁶ Creative Electronic System S.A., Route du Pont Butin CH-1213 Petit Lancy (Switzerland)

⁷ We used the line T10 ($5 \text{ GeV}/c \pi^-$ beam) of the East Hall.

⁸ Configuration and performances for the 2 CPU boards are very similar: the test program we used was recompiled without modification and ran at the first time.

⁹ This number refers to an event with all 4608 pads turned on.

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