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POWER SUPPLY SYSTEM FOR THE TRACKER DETECTOR OF THE AMS EXPERIMENT

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Power supply system for the tracker detector of the AMS experiment

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Abstract

The AMS experiment is devoted to the measurement of the antimatter component of cosmic rays in particular the detection of anti-nuclei. The apparatus will operate in space. A preliminary version will fly in 1998 on a Space shuttle mission. The complete system will be installed on the space station Alpha in 2001. The apparatus, in its complete version, will be composed of a magnetic spectrometer based on a microstrip silicon tracker and on a permanent magnet. This instrument will measure the momentum and the magnitude and sign of the charge of the incoming cosmic ray. A time-of-flight detector will be used as a trigger, for up-down rejection and for the measurement of velocity for low-energy particles. A threshold Cherenkov detector will provide further up-down discrimination. An anti-coincidence system, placed on the lateral inner wall of the magnet, will provide suppression of the background due to interaction of primary cosmic rays with the magnet. A transition radiation tracker will identify electrons. This paper describes the power supply system for the tracker detector giving also a short description of the tracker detector electronics to be powered. Results of preliminary tests and studies are also reported.

I. The AMS apparatus

The AMS experiment [1] is designed to measure the antimatter components of the cosmic rays, in particular anti-nuclei, with a sensitivity of 10^4-10^5 better than the current measurements. It will also measure the:

- Positron spectrum from 0.1 to 100 GeV.
- Antiproton spectrum from 0.5 to 3.0 GeV.
- Gamma ray spectrum from 0.1 to 300 GeV.
- Deuterium flux from 1 to 3 GeV.
- Isotopic composition of Helium and Beryllium from 1 to 3 GeV.

The apparatus (Fig. 1) will be composed of:

1. A permanent cylindrical magnet equipped with 6 planes of microstrip detectors with expected space resolution better then 10 μm in the direction of bending. The magnet will deflect the charged particles to detect the momentum (measurement of the bending radius) and sign of the charge (direction of bending). The residual induction of the magnet is around 14.5 kG and the expected resolving power is 0.15 Tm^2 . In addition the Silicon detectors are read by a wide dynamic range electronics for the determination of the charge absolute value which will be possible for nuclei up to $Z \approx 20$.

2. A time-of-flight system based on 4 planes of scintillator detector having about a 100 ps time resolution. This detector will be used to trigger the apparatus, to measure the velocity for low energy particles, to contribute to the suppression of upward moving particles and to give a measurement of the charge absolute value.

3. An anti-coincidence veto counter (Ai) will provide the rejection for particles coming from secondary interaction with the wall of the magnet.

4. Two Cherenkov detectors: C1 and C2. C1 will provide β measurement and C2 will reject the upward moving particles (in conjunction with the time-of-flight system).

5. A Transition detector tracker. This instrument will be used for the identification of electrons. Within this detector a layer of tungsten having thickness of 1 mm will be included to convert cosmic gamma rays into electron-positron pairs to be further analyzed in the spectrometer. This detector will be segmented into 3 parts: one over the converter and the magnet, one between the converter and the magnet and one under the magnet.

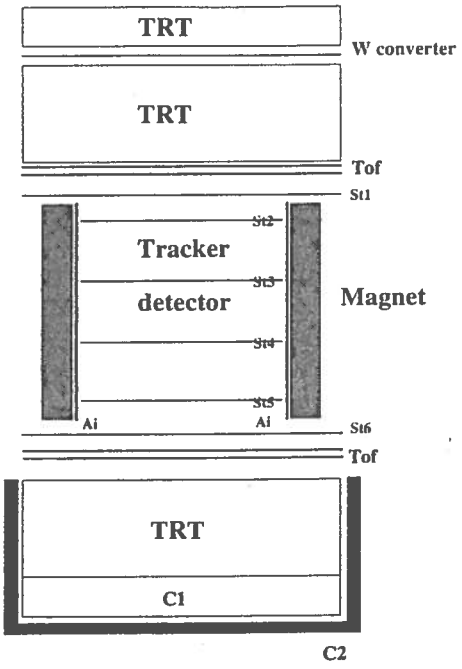

Fig. 1 The AMS Apparatus

II. Overwiev of tracking readout electronics

The tracker detector for the AMS experiment is made of 6 Silicon detector planes; 4 are located inside the inner volume of the permanent magnet, one is over the top and one is below the bottom. The tracker is built from Silicon sensors. Sensors for the AMS tracker have the following dimensions: 70 x 40 x 0.3 mm^3.

The sensor is segmented into strips on both sides. On the p-side the strip pitch is 55μm and on the n-side is 52μm; the p-side is segmented into about 1270 strips (along the 70 mm side) and the n-side into 767 strips (along the 40 mm side). The strips on both sides are directed orthogonally. Each sensor also has a guard ring, its polarization being achieved by connecting the guard rings on both sides to a biasing potential. The guard ring on the p-side is connected to each strip by 10$G\Omega$ resistors, while that of the n-side is connected to each strip by a 40$M\Omega$ resistor. When biased a sensor draws an average current of ca. 400 nA, 2μA maximum.

Silicon sensors are assembled to form a ladder. A ladder is a row of detectors with strips bonded on the long (70 mm) side. Depending on the structure of the tracker, a ladder can be composed of 7 (280 mm long ladder) to 15 (600 mm long ladder) sensors. The n-side of a ladder will be glued onto a Upilex [2] (similar to kapton) cable connecting the strips together. The n-side is sometimes referred as the K-side while the p-side is called the S-side. Metal strips on the cable will ensure the connection on the K-side. The biasing potential is +48.8V, applied on the K (n) side.

The readout of the ladder is accomplished by several 64 channel chips called VA_hdr. The chips are glued and bonded on a hybrid substrate. This front-end hybrid card is called the TFE (Tracker Front End). There are 10 chips reading the S-side (p-side) connected with one channel every two strips (readout pitch of 110μm) and 6 chips for the K-side of each ladder. The readout pitch on the K-side is 208μm (one channel every 4 strips). With this chosen number of readout channels (384 per ladder) in the K-side it is not possible to read all the strips individually. For this reason every readout channel is connected to $d/2$ strips where d is the number of detectors on one ladder. In this way we introduce an ambiguity on the non-bending coordinate to be resolved during the construction. The VA_hdr chip includes a low noise CMOS charge preamplifier, a CR-RC semi-gaussian shaper, a sample-and-hold and an analog multiplexer. The readout of the S-side of a ladder proceeds along two independent output lines, one for each 5 VA_hdr chip. On the K-side only one output line (for 6 chips) is implemented. The VA_hdr is connected to the silicon strips through a decoupling capacitor chip that is not able to withstand the applied bias voltage; the readout for the K side has therefore to be referred to a voltage close to the biasing potential. On a TFE we have also the receiver circuit for the digital signal and several filters.

The front-end electronics requires $\pm 2V$ and a reference ground voltage with a long term stability of $\pm 50mV$. The power consumption of a VA_hdr chip depends on the prebias current. We assumed a power consumption of $0.77mW/ch$ which correspond to a total power consumption of $45mW/chip$. Currents drawn by the chip will come to a total of 24.58 mA; about 20.05 mA from the -2V input and 4.53 mA on the +2 V input at 250μA prebias current. The reference ground voltage for the S (p) side will be 0 V while for the K (n) side it will be +50 V. The biasing voltages for the detectors will be referred to the same ground reference. For the p-side (dVp) the bias voltage will range from -2 to -7V. For the n-side it will have the fixed value of -1.2V (dVn) in addition to the reference +50 V. The ladders will be assembled into planes. The ladders in the inner plane have a length varying from 280 mm (7 sensors) to 520 mm (13 sensors) The TFEs will be bent by 90^0 with respect to the detectors and connected to the detector such as to minimize the space occupancy within the magnet. Outer planes St1 and St6 contain longer ladders (up to 15 detectors i.e. 600 mm) because they are allocated outside the inner volume of the magnet. A total of 172 ladders is foreseen for the entire detector.

III. The AMS Tracker Power Supply System

The power supply cards for the AMS detector will be integrated inside the electronic crates which will also be used for readout electronics. The readout electronics and power supply crates for the entire experiment will

be placed around the magnet structure. The crates are VME 6U having 19 slots (long crates) or 8 slots (short crates) with a custom backplane. For the entire tracker detector 6 long crates will be allocated; one for each two half planes.

Each crate has is own power supply; for the tracker crates it will be named PSCT. Each PSCT will contain DC-DC converters from Modular Devices Inc. (MDI), that will provide a 5.2V output for powering the control electronics. The backplane of the crate will also include a double-redundant +120V line from the main power supply of the shuttle or space station. The readout of the tracker will be accomplished by the TDR cards (12 per crate 8 ground-referred and 4 bias-referred) and a JDQT controller for each crate that reads the TDR cards and formats the data for further processing and transmission. A TDR card contains:

- 8 analog receivers
- 8 ADCs
- 4 DSPs (2 active and 2 redundant)

The cards having input and power referred to the bias voltage (TDRKs) are divided into two halves (galvanically separated) and have optocoupler output circuits in the connection to dataway because they are connected to the JDQT that is not referred to bias. A TDRS is connected to 4 half-ladders (the side of a ladder referred to 0 V) receiving the output of 8 output lines. A TDRK is connected to 8, 50V-referred half-ladders and also receives the output of 8 output lines. The central 6 slots of each tracker crate are allocated for the power supply cards. The 6 cards located in the crates are arranged as follows:

1. 1 TBS (tracker bias supply) provides the bias for the detectors (dVn, dVp) and the reference ground for the electronics in the non-bending side (K or n side). It will take power from the 120 Volts primary line and +5.2V from the PSCT for the digital control electronics. Power output is negligible and power dissipation about 5 W.

2. 4 TPSFEs (tracker power supply - front end) provide power for the front end circuits. Each card will power 8 front-end circuits (full ladders K and S side). It will take the +120 V primary line, the bias voltage from the TBS and +5.2 from the PSCT for the digital electronics giving ±2 volts and a ground return for both the S-side and the K-side. It will have 6.4 W of output power, (assuming 55% efficiency), 11.6 W input power and 5.2 W internal dissipation.

3. 1 TPSR (tracker power supply - readout) provides power for the readout electronics; each card will power 12 TDR cards, 8 referred to ground (TDRS) and 4 referred to bias (TDRK). It will take power from the +120 V input voltage primary line, the bias voltage from the TBS and the +5.2 Volts for supplying the control logic from the PSCT. The output voltages will be $\pm 6V$ (unregulated) and ground return. The output power for this card is 39W, assuming an efficiency of 76%; the input power will be 51 W with an internal dissipation of about 12 W.

The power supply cards are connected to the TDR through the custom backplane bus and not directly to the front-end electronics since cables are foreseen only between the front-end and the TDRs.

At the beginning of this project various architectures were foreseen for the different PS cards but most of them have proved not to work on a magnetic field larger than 50 G. Since the magnetic field in the region of the PS cards varies from 100 G to 272 G, the entire project had to be redefined.

The monitoring system is based on the CAN protocol, its controller being housed inside the JDQT. The control and monitoring circuit will be described in a specific paper.

IV. The TPSFE

The TPSFE card provides power for the 8 full TFE (hybrid) circuits. Its output voltage are: ±2 volts (regulated) and ground (referred to 0V) for the S-side and ±2 V (regulated) and ground (referred to +50V) for the K-side. A TPSFE will provide a total of 48 (3 x 2 x 8) separate output voltage lines. This card can be divided into three sections:

1. a switching power supply section.

2. a linear regulator section.

3. a control and monitoring section.

The switching Power supply we have adopted is based on an integrated current flyback switching power supply by Modular Devices Inc. model 3315, especially designed for the AMS experiment. It is a custom-made hybrid enclosed in an Iron shielding box. It accepts on the input a voltage between 86 and 158 VDC and has a dual output of $\pm 2.6V$ with common return line. The typical output ripple is 50 mVpp (max 85 mVpp), the quoted efficiency is about 75% and the maximum output power is 5.5 W. Each module can give a maximum current of 1.6 A on -2.6 V and 0.5 A on +2.6 V. The circuit in the hybrid includes [3] (see block diagram fig. 2) a common mode filter on the input line, a two-stage LC input differential filter, a current flyback DC-DC converter with a highly compact transformer, an LC differential filter and a common mode filter on the output lines. This circuit is guaranteed by the manufacturer to operate in a maximum static magnetic field of 500 G. This performance have been tested within the AMS collaboration by ETH Zurich. No change in efficiency and output ripple was observed in the static magnetic field range from 0 to 500 G. Additional attractive features of this module are: operating temperatures at

full efficiency -55^0C to 85^0C, with linear derating up to 115^0C, shock resistance up to 50 g, acceleration resistance up to 500 g and vibration resistance up to 30 g.

Each TPSFE card will contain a total of four MDI-3315 modules per card; two of them will power 8 S-hybrids and two 8 K-hybrids. Since this module operates at a typical output power (for the supply of S-side hybrids) of 2.6 W, much below their maximum capability, their failure rate will be very low and no spare modules are foreseen in any of the TPSFE cards.

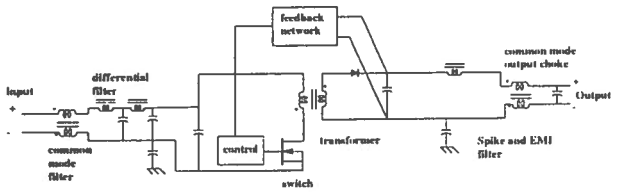

Fig. 2 Block scheme of a hybrid DC-DC converter

The outputs of the switching DC-DC converters goes to the low-drop linear regulators. There will be four (one for the +2 V referred to ground, one for the +2 V referred to bias, one for the -2V referred to ground the and one for -2 V referred to bias outputs) regulators for each ladder supplied for a total of 32 regulators per TPSFE card. A linear regulator section also includes a foldback current limiter; the current limit of the foldback is placed at 3/2 of the expected current. The regulator and current limiter for the TPSFE for a +2V output for the S-side is shown in fig. 3. The regulating transistor Q2 is driven by an operational amplifier (U1A in the drawings) that sets its output current in such a way that the non-inverting input (connected to the regulator output) has the same potential as the inverting input which is held at +2V by a voltage reference. When the overcurrent on resistor R33 occurs U1B and D2 brings U1A into positive saturation, thus limiting the current on Q2.

The behavior of an MDI DC-DC converter in connection with this linear regulator has been tested and simulated. The output ripple of the +2V regulator shown, connected to a dummy load simulating the current drawn by 10 *VA_hdr* circuits, has been measured with a Tektronix Mod 2252 and its amplitude was 0.8 mVpp. The input ripple was 10 mVpp. The contribution of this ripple with the total noise on a TFE prototype has been measured comparing the output noise from a TFE supplied with this system with the output noise from the same TFE connected to a power supply built from batteries. The difference was found negligible.

The ripple was measured for the negative regulator too, and had the same value.

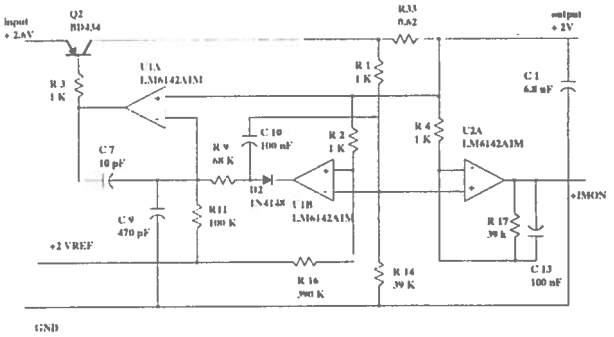

Fig. 3 +2 V linear regulator schematics

V. The TPSR

The TPSR provides ±6V (unregulated) and ground level referred to 0 V for 8 TDRSs and ±6V (unregulated) and ground level referred to 50 V for 4 TRDKs. It takes the power from the +120 V primary line. The card is divided in two halves:

- The ±6V converter section for the S side
- The ±6V converter section for the K side

Like the TPSFE, this card too includes its control and monitoring circuitry.

Also in this case flyback DC-DC converters from MDI will be employed. For the S section a modified version of the 3051M-T06, named 3318, will be used. The maximum output currents for this module are: 4.2 A on +6V and -0.8 A on -6V. The ±6V converter section for the S side is composed of 2 (1 active 1 spare) of these modules. Voltage regulators producing ±5V will be placed inside each single TDRS board.

The ±6V converter section for the TDRK is composed of 8 active modules with no spares since they are used at below half of the maximum power they can provide. These modules are MDI-3317 derived from 12578M-D06. They can provide 0.624 A on the +6V line and 0.084 A on the -6V. Each of these modules powers half a TDRK. Each module has its ground referred to the 50 V bias.

The output power for this card is 39W; assuming an efficiency of 76% the input power will be 51 W with an internal dissipation of about 12 W. Since the power dissipated has a very high value, a detailed thermal study of a preliminary version of the layout of this board was performed. The result of this study is that if a dissipation layer of thickness 0.46 mm is used, the temperature of the components are around 10^0C above the crate temperature.

VI. The TBS

The TBS (tracker bias supply) provides the bias for the detectors (dVn, dVp) and the reference ground for the electronics in the non-bending side (K or n side). Each card will supply 32 ladders and provides areference bias

to 4 TDR cards. This card will take power from the 120 V primary line and the 5.2 V power lines of the PSCT for monitoring and controls. It will produce the following voltages:

dVp Variable voltage from -2V to -7V. This is used to bias the guard rings of the p-side of sensors on 32 ladders.

dVn Fixed voltage -1.2 V. This is used to bias the guard rings of the n-side of the sensors on 32 ladders.

Vgref Provides ground reference (at +50V) for 4 TPSFEs, 1 TPSR, 4 TDRs (TDRKs).

The switching DC-DC converters are MDI-3316 derived from MDI-3060M-T9. They can provide +60 V with a maximum current of 0.2 A and -9V with a maximum current of 0.12 A. In each TBS we have two of these modules both working at less than half the maximum current they can provide. Because of this implemented redundancy, if one of the two DC-DC converters fails the other can provide the current for the entire card. A block scheme of this card is given in fig. 4. The two DC-DC converters are connected to two sets of linear regulators.

The first set is connected to the +60V output of the DC-DC converters through diodes and is composed of 8 independent regulating units each having 4 dVn outputs (+48.8 V) and 1 Vgref output (+50V).

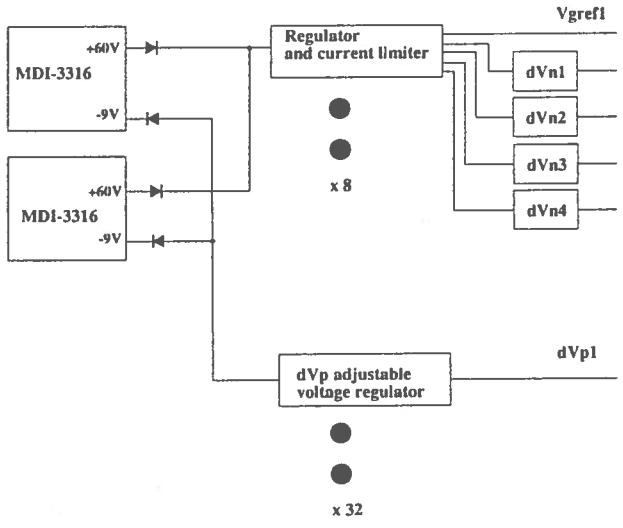

Fig. 4 TBS block diagram

Each unit includes a voltage regulator, a current limiter, a circuit for reducing the output voltage to +25 V for Vgref and +23.8V for the 4 dVn, and 4 independent output stages for the dVn outputs.

The second set of circuits is connected to the -9V outputs of the DC-DC converters and is composed of 32 independent voltage regulators for the generation of the dVp voltage which can be adjusted via commands from the control circuit from -2V to -7V.

VII. Conclusions

In this paper we have described the tracker power supply system architecture of the AMS apparatus in connection with the electronics circuits and detectors to be powered. The power supply system includes control and monitor circuits not described in this paper. Ripple measurements for the TPSFE circuits and the results of a thermal simulation on the TPSR card are also reported. All cards described in this paper are currently under construction and will be integrated within the crates on the AMS tracker electronics starting in march 1997. Before the integration, the cards will undergo about 200 hours of burn-in and successive thermo-vacuum and vibrational tests to prove their reliability to be used in space.

VIII. References

[1] R. Battiston Nucl. Physics B (Proc. Suppl.) 44 (1995) 274-281.

[2] Upilex is a Trade Mark of IBM, ENDICOTT. New York (USA).

[3] Hybrid DC/DC converter Aplication Notes. 2nd edition. published by Modular Devices Inc.