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CHARACTERIZATION OF LARGE SERIES OF DOUBLE SIDES SILICON MICROSTRIP DETECTORS

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Abstract

We describe extensive tests performed for the first time on a very large series of double sided silicon microstrip detectors. We discuss the testing methods in terms of time and reliability and the special procedures to test both the p and the n sides. The results show an excellent performance on a long run for the production of double sided silicon microstrip detectors.

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1 Introduction

Many experiments make use or are equipping with microstrip silicon detectors. In particular current collider experiments are upgrading with new silicon vertex detectors. At the future facilities, like B factories, in KEK, SLAC and Cornell, experimenters are now designing their detectors. There are options for microstrip detectors and pixel detectors, still realistic in terms of radiation hardness. For the future high luminosity LHC experiments, or for the upgrades of the Tevatron experiments D0 and CDF, many layers of silicon microstrip detectors will be needed to perform the tracking as close as possible to the interaction region. The dimensions will require a very large number of microstrip silicon wafers to reconstruct coordinates both along the beam axis and transversal to the tracks. For these measurements, several options exist and have been exploited in current experiments:

- glue two sensors together, each with single side implanted microstrips in orthogonal directions [1];
- use double metal readout on single or double sided implanted orthogonal microstrip detectors [2];
- use double sided microstrip detectors with implantations in the opposite faces of the same wafer and in the orthogonal directions.

So far, little is known on the behavior on large scale and long run of double metal detectors, while experience is being gained on large scale production and running of double sided silicon wafers. In addition technique to read out both sides of the detectors without sensibly increasing the radiation length, have now been proven to be reliable [3]. For these reasons the double sided detectors, look more appealing than the single sided ones, provided the costs in terms of money and manpower, for the construction of the wafers and the testing are kept comparable. Although the double metal solution looks more elegant, at present the costs and the reliability in large scale needs still to be worked out.

So far the double sided detectors have been used only in two experiments [4], [5], after years of development on an original design [6] and they are now being part of the upgrades of existing vertex detectors [7]. On the basis of the experience now being acquired, the double sided silicon microstrip wafers are considered as definite

options for tracking at future experiments [8]. In particular for the large high energy physics experiments, it is extremely important to advance on the large scale structures under many aspects: in this paper we descri be the experience we have acquired in terms of fabrication and testing of large series. We critically review the relevant quantities for the certification of (double sided) silicon sensors; we describe in details the measurements set up and we finally report the results on a large number of silicon wafers. We give explicitly the failures rates for each step from the wafer fabrications to the final tested detector: this will help to give realistic estimates of the costs, in terms of manpower, time and money for the choice of double sided microstrip detectors. We show that the fabrication and the tests in large series can be performed in a fast and reliable manner, indicating the double sided detectors as excellent candidates for the next tracking devices in high energy physics and other large scale applications.

2 The detectors

The detectors (figure 1) were fabricated[2] on common detector grade high resistivity silicon wafers[3] of n-type. The details on the measurements of the resistivity are described in section 4.2.1. Here we simply mention that the large majority of the doped silicon wafers showed excellent quality, with very high resistivity values, far above the needed specs.

The detectors had orthogonally implanted strips on the two sides of a silicon wafer: of p^+ type (figure 2) on one side and of n^+ type (figure 3) on the opposite. In this case, special back-polishing [4] had to be done, as implantations are in both sides. The measurements of the thickness on a large number of wafers, reported in 4.1, gave fairly constant values with a typical value of 310μm including the oxide thicknesses.

The wafers were processed[5] in both sides in a familiar way[10] with junctions realized by B implantations in the n bulk (the p^+

[2]CSEM Neuchatel Switzerland
[3]formerly Wacker Che. Burghausen Germany
[4]Von Ruse Ent. INC. Caldwell IDAHO USA
[5]Processing by CSEM and design by INFN-Pisa

implantations), after the deposit of the silicon nitride on the oxide grown at the two surfaces and the photolithography etching. The shapes of the implantations were different: in one side (side *I* or p^+ here for convenience)[6] the strips were straight for a 70400μm length, they had 10μm width, 1μm thickness and 25μm interdistance (pitch). On the opposite side (side *II* or n^+ here) the p^+ strips were in the orthogonal direction, straight for a length of 34800μm but with a "u-like" biforcation at the two extremities for a length of 495μm, 10μm width, 1μm thickness, at 50μm pitch. In this very side it was then fabricated, after photolithography etching, another structure of n^+ type by P implantations in the n bulk for a length of 34000μm, 10μm width, 1μm thickness and 50μm pitch. Passivation, via oxide deposition, was made on both sides and finally the photolithography etching for the Al contact windows on the p^+ implantations only on side *I* and on the n^+ implantations on side *II*. The Al strips were realized by deposit and photolithography etching at side *I* for 70400μm length, 12μm width, 0.5μm thickness, at 25μm pitch, with bonding pads at both edges for a length of 200μm, 50μm width; while at side *II* 34800μm length, 12μm width, 0.5μm thickness, at 50μm pitch, with bonding pads at both edges for a length of 200μm, 50μm width; the pads were alternate. As described elsewhere [6] and partly demonstrated in the tests reported later in section 4, this innovative design in the side *II*, for the measurement of a second coordinate in the same wafer, gives excellent performance [11].

Both sides were equipped with guard rings. Side *I* had two guard rings to reduce further possible effects of surface currents (see section 4.3): they were both made of 95μm width p^+ implantations, with 100μm Al width, at 10μm pitch with the inner at 5μm distance from the outermost strip. Side *II* had only one n^+ implantations as guard ring, with 500μm width, at a distance of 500μm from the ends of the n^+ strips, which corresponds to about the length of the "u" at the edges of the p^+ strips, the extremity of which are at 5μm from the guard rings. In the direction parallel to the strips the guard ring is at 50μm from the outermost strips.

[6]It is frequently indicated as p or p^+ or *junction*side. Similarly the opposite has been often called the n or n^+ *ohmic* side. Given the peculiar design presented here, this terminology is not followed as it would be misleading.

The detectors can be read out by inverse biasing with a positive voltage (with respect to a common ground) the guard ring in the n^+ side. In the opposite, a voltage drop is created via a punch through current, between the strips and the guard ring [12].

Before the tests, the wafers were cut with a diamond dice, separating the detectors from the test structures. The very large number of cuts, were well within the specified dimensions. This was very important for the tests set up described in next section, since we could keep the same mechanical equipment for all the series tests, without having to modify it, saving the time needed for each test as described in section 5.1. Table I summarizes the geometric characteristics of the detector.

3 The set up

For a certification of a large series of detectors, the requirements for the tests were very stringent. They had to be as much as possible: fast, reliable, reproducible, simple, of immediately interpretable answer. These requirements were translated in a test set up which had to compromise extremely delicate and, at the same time, precise mechanical operations, with very accurate electrical measurements. Any tiny mechanical movement could strongly influence the measurements, if not seriously damage the detectors. To give an example, a simple tight bending of a cable probing the current of a single strip, could give variations orders of magnitude larger than the value to be measured.

Correspondingly, to control possible external influences [9], all the tests were performed in clean room.

In the following we describe the mechanical tools and the jigs built. The accurate instruments and their peculiarity for our measurements are described in section 4.

3.1 The tools

To precisely probe the detectors and the test structures, we mounted them flat in a Karl Suss[7] probe station model k400/PM8 (figure

[7]Karl Suss Germany

4) equipped with several probe heads with vacuum and mechanical supports (type nm340, nm350). The heads connected the probe tips (type Karl Suss 34 of tungsten, 8μm diameter) via coaxial internal connection, to the triaxial cable, plugged to the electrical instruments. For one shot measurements of a large group of strips, we have used a probe card[8] equipped with 60 needles (tungsten, 8μm diameter), with a 50μm pitch. The card was plugged to a fixed 60 pins connector, with corresponding 60 triaxial cables soldered on the other side. All that was mounted in a support which had to be very planar and fixed to the station: this was important as the detector was slide below, with an excursion of 4000μm in the transversal direction. If well planar, at each displacement the focus of the microscope to monitor the probing could stay fixed and the force of the tips constant, without risk of damaging the probing pads nor of improper electrical contact: this helped to reduce the number of operations, saving time on series tests and diminishing the risk of damages. Additional special mechanical jigs were used for the contemporary probing of the two sides. In most of the measurements the bias was brought from the back plane and the tests performed on the top surface, as shown in figure 5: a tip was mounted on a special head with adjustable cursor; for operations on it the jigs had to be taken out of the probe station and moved to a separate microscope (a different approach but with similar solution in [13]). The jig was then fixed with fast screw to the probe station support.

The probe station was contained into a large aluminum black painted box (visible in figure 4), reducing light collection into the detectors, to disentangle from it other leakage current contributions. From this box, in which permanent triaxial connectors are fixed, other triaxial cables go to the instruments. Special care was devoted to the grounding, making sure that there was only one common ground on the box as well as on the chassis of each instrument.

3.2 The electrical instruments

The quantities to be measured for a certification of a silicon detector are discussed in details in section 4, here we simply recall them to

[8]Wentworth Lab. Munchen Germany

better explain the use of each instrument.

For this type of double sided detectors we had to determine:

- the overall leakage current;
- the single strip leakage current;
- the bulk capacitance;
- the interstrip capacitance;
- the interstrip resistance;
- the punch through voltage.

All these quantities or their variations, are typically very tiny. As an example we simply mention here that a typical single strip leakage current was of the order of 100pA, therefore, assuming the measurement had to be performed with at least 1% accuracy, the instrument must had a precision of 10^{-12}A. In addition the stability had of course to be at most of the same order.

The instruments we have used, are listed below.

The Keithley *237*; a femtoaperometer used as voltage source, sensing the current for the leakage current measurements, with read-out cycle of 32 readings/sec, free scale. We also used it as current source and voltage measurement of the punch trough voltage.

The Keithley *590*; a capacimeter used in alternate mode to send the signal to sense and then measure back the capacitance values.

We used also the Keithley *595*, a static capacimeter, and the Keithley *237*, simply as additional voltage sources.

The Keithley *707*; a multiplexing unit which allowed low noise and fast switching from different current and voltage sources and sensing units.

Different settings and measurements were driven by computer without changing the hardware set up, with as many as 70 different connections activated and/or switched at the same time, with response at most within less than a second. This was fairly sufficient for the serial measurements: as an example the single strip measurement, performed on one shot of 56 strips, needed anyway the reading cycle time to be stable before each acquisition, waiting for the same time interval. All these switching operations didn't at all influence the noise level in the measurements, irrespective of the speed and of their amount. The connections set up was different for the different measurements and it was changed accordingly,

intervening on the *707*, mainly via software.

All the instruments had a serial GPIB interface which received the computer commands, with easy programming.

With this set up, we avoided cabling changes during the serial measurements. This allowed us to run with sufficient speed and to reduce faults.

Hardware interventions, although as simple as cables plugging and probe tips movements were done only in the case of sampling measurements.

To illustrate the general scheme a sketch is drawn in figure 5, the detailed set up is described in section 4 for each measurement.

4 The measurements

In this section we give the details of the measurement procedures and we critically review the relevant quantities for the certification of a double sided microstrip silicon detector. We then describe the large series tests, reporting the overall results for each single quantity.

To start with, we first report on the mechanical failures.

4.1 Mechanical controls prior to the tests: polishing, processing, dicing

The number of wafers delivered by the fabrication company are as many as ordered, without failure allowances, i.e. there are in principle no faulty wafers delivered. On the contrary when going to the polishing and to the fabrication and dicing processes, some failure arises. This counts at the expenses of the total failure rate.

Here we report only on the measurement on the external dimensions of the detector, performed to check the wafer thickness after polishing and the dicing accuracy. The failures for processing and ruptures during it, are more extensively reported in section 5.2.8.

The specifications for the final thickness after back-polishing were: $(300\pm10)\mu$m. The measurements, sampling on a large number of wafers, gave fairly constant values within the error: a mean value of 315μm with an instrument error of $\pm$ 3μm and an r.m.s. of 8μm, all after full processing, including therefore the deposition thicknesses.

The maximal difference within the same wafer was measured to be 15μm, i.e. the wafers can all be considered flat within the errors and in accord with the specs.

The typical failure rate, i.e the number of wafers which were unusable after polishing, was very small: $12/300 = 4\%$. The wafers were processed in batches of 24: typically very few wafers didn't reach to the end: over 12 batches 89% of the wafers reached the end of processing and they were delivered. In 4 cases only, over 255, the wafers were damaged by the cut. These excellent results are summarized in figure 6.

4.2 The bulk capacitance

The detector works overdepleted. To operate it, one has to determine a priori the reverse bias voltage at which the junction depletes. In order to do that, one can measure the capacitance in between the two junction electrodes. Since this is difficult in hundreds of microstrip detectors, as one should then account by all possible neighboring structure effects (guard rings and strips), we have measured the *bulk capacitance*, often called the *back plane capacitance* or the *body capacitance* C_b, on a test structure fabricated on purpose on each wafer. This procedure is frequently used. We underline that the assumption which must be done is that the wafer is homogeneous, in particular under the surface of the detector implantations, in terms of the resistivity (indirectly measurable) or of the doping concentration.

To have an a priori determination of the resistivity, one can either enter the doping concentration, if accurately known from processing,

$$N_d = \frac{2\epsilon \times V_d}{e \times {t_d}^2} \tag{1}$$

$$\rho = \frac{{t_d}^2}{2\epsilon \times V_d \times \mu_e} \tag{2}$$

with:
V_d depletion voltage;
μ_e *drift mobility* or often simply *mobility* for electrons $=1350 cm^2/Vs$;
e electron charge;

N_d doping concentration, i.e the fraction of majority carriers atoms in the silicon crystal (in this case the Phosphorus);

ϵ, dielectric constant of Silicon $=106.248 \times 10^{-12} F/m$;

t_d= depletion thickness of the diode.

Or, alternatively, one can determine the resistivity via the C_b and V_d measurements (see discussion in next section 4.2.1).

Taking the thickness of t_d=315μm (section 4.1), the equation 1 gives $N_d = 4 \times 10^{14} charges/m^3$. This value, calculated taking the experimental mean value of depletion voltage (4.2.1 and figure 8) of 24volt, can be cross checked with the measurements on the capacitance and on the resistivity, presented later viaequation 3:

$$C_b = \frac{\epsilon \times A}{t_d} \tag{3}$$

with:

A, area of the implantation, $= (0.1 \pm 0.01) cm^2$.

With the present state of art, the uniformity of the resistivity is of the order of 1%/mm[14], as a radial variation. This is the order of magnitude by which the absolute value of the bulk capacitance has to be considered. Anyway the important check is to evaluate that it is substantially smaller than the interstrip capacitance C_{ss}, to loose the minimum amount of charge and therefore not to deteriorate the resolution (see also later the discussion on C_{ss}) and that it is constant for voltages higher than depletion.

In summary the measurement on the bulk capacitance had to verify that it was:

- as constant as possible in the widest possible bias voltage range;
- directly proportional to the resistivity in a linear way;
- as small as possible with respect to the interstrip capacitance;
- its absolute value within expectations.

In addition we have also verified the homogeneity of the values for all the wafers as for the other parameters. This is described in section 5.2.2.

The set up, to perform the measurement on C_b, is shown in figure 7. The test structure, separated from the detector at the dicing phase, is mounted in a jig different from the one used for the other detector measurements. The measurement is performed biasing the

n^+ back plane with reverse voltage variable from $0V$ to $+70V$, while sensing the top and probing and polarizing the inner guard ring. The connections to the *590* pass via the *707* with triaxial connections. The program gives a start to the *590* meter which sends a signal of frequency of 100kHz and amplitude of 15mV r.m.s. it then measures the return signal phase with an accuracy of 0.1ns, which, with the scale set, gave a fair accuracy on the capacitance measurement of 1fF.

A typical C_b curve is shown in figure 8. The value after the knee is 3.560pF. A further check on its absolute value can be done by calculating the expected capacitance from the dimensions of the test structure. This is done in the next section.

4.2.1 The resistivity and the depletion voltage

At the knee of the curve of figure 8, the junction depletes: the corresponding depletion voltage value V_d is determined from the intersections of the two extrapolated portions of the curve via least squares fit. As compared later the value of the bulk capacitance is lower enough with respect to the interstrip capacitance, to expect charge division readout working. It can be noticed that the V_d is quite small and this guarantees, as shown for the leakage current measurement, a safe detector operation while overdepleted. Actually full depletion of the detector, given the several complicated structures, is hard to reach. There are several contributions to the currents flow which we discuss later and which indicate that not all the p^+n neighborings are fully depleted at V_d.

The fact that the resistivity is so high implies that the leakage current is low and the doping concentration of the bulk n crystal, high enough. The values are reported in figure 8 and can be cross checked with equation 3, showing agreement with expectations.

For these detectors the test structure was a circular diode of radius $r_d = (1700 \pm 30)\mu$m with two concentric guard-rings at a distance of 50μm each. Assuming the thickness is the mean value of the ones reported in section 4.1 ($t_d = 315\mu m$), via equation 3 with an area of the implantation as full inner circle of the test structure $9.1 \times 10^6(\mu\text{m})^2$, one can deduce the expected capacitance $C_b = 3.1pF$.

Viceversa one can deduce the depletion thickness of the junction

to verify how deep the depletion reached, by taking the asymptotic value of the capacitance at full depletion from figure 9, $C_b = 3,560pF$. This gives $t_d = (277\pm10)\mu$m, in agreement with the mean measured value of the thickness, indicating that the full junction was depleted.

The plots in figure 9 show the cumulative distribution of the resistivity for few processed batches. These do not necessarily correspond to the same silicon wafers production batches; this therefore gives a definite indication on the spread over the all series. A similar distribution for the depletion voltage is shown in figure 10. The mean value is pretty low: (24.0 ± 0.8)V with an r.m.s. of 8volt. This is relevant for the quality of the detectors as for the case of the resistivity. The fact that the spread is limited is very important for the operation of the detectors when assembled together: this allows similar operation voltage values of all the detectors. Since one usually pairs them, this fact also eases handling operation, assembly and running. To guarantee that the detectors could function highly overdepleted, we have performed all the measurements described below at $1.5 \times V_d$ (which we call the *operation voltage* V_o) and eventually at $2 \times V_d$ or higher.

To compare, via equation 2 the values obtained for the resistivity, using the mean V_d of 24.0volt, we obtain a mean expected resistivity of (11.6 ± 0.4)kΩcm, in agreement with the value of figure 9 of 14.5kΩcm.

4.3 The leakage current

The leakage current of silicon microstrip detectors is the main source of the noise. It is therefore necessary to determine it with great accuracy and certify the detectors mainly on the basis of its values. Nowadays the detectors technology has reached high quality standards. In addition even if commercial electronics has now very low charge collection thresholds, the noise contribution, in terms of equivalent noise charge injected from the detector into the preamplifier readout, due to the *dark* or *leakage* current, must be relatively low. We then expected low values of leakage current and we had to detect tiny variations which indicate fabrication defects.

We distinguish the sources of high leakage current as listed below.

1. The generation current I_g

This is due to the presence of the minority carriers into the crystal which, at the wafer fabrication phase, can't be further reduced below a very low doping concentration as indicate the resistivity measurements. According to the expectations:

$$I_g = \frac{e \times n_{Si} \times t_d \times S}{2 \times \tau_g} \tag{4}$$

with

n_{Si}, intrinsic carrier[9] density of silicon $= 1.5 \times 10^{10}$;

τ_g, generation lifetime $= 20\mu$sec [15];

S, the detector active area taken within the guard rings $= 230 cm^2$ (see section 2).

This gives $I_g = 20\mu$A.

Strong deviations with respect to the expectations from equation 4, indicate defects of the crystal bulk, which might be due to wrong manipulations bringing to mechanical cracks, even invisible to naked eye inspections. This might be typically the case of improper dicing and we have observed some cases at the very beginning of the large series production, which we could attribute to imperfect setting of the dicing machine. This is only an example of how the I_g can assume high values. Another case could be wrong fabrication processes, like defective implantations.

2. The surface current I_s

This is the name given to migrations of charges as a function of time, with very little depth (few μm) because of local electric fields between implantations and implantation-oxide. The charge can be momentarily trapped in the oxide or it can accumulate in the vicinity of an implant. Usually the guard ring (for our detectors two in the p^+ side) limits considerably, if properly polarized, such a current. Defective implantations or aluminizations, can create high local electric fields to move the free charges from, over or into the implantations, depending on the sign. These sum up to give a

[9] The electrons are the carriers. Minority carriers if we consider the reverse polarized p^+n junction for the leakage current in the p^+ side. The electrons are majority carriers if we consider the leakage current in the n^+ side. The different behavior is described on section 4.3.2

net current which can substantially contribute to the total leakage current as discussed below.

4.3.1 The total leakage current

Although we have said that there are distinct contributions to the leakage current, the measurement which can be done is limited to what we will call *the total current* I_T of the detector, i.e. the one measurable between a guard ring in the p^+ side and the guard ring in the n^+ side. For the series certification of the detectors, this is fairly good indicator of imperfections. The net current measured is the sum with the signs of all the contributions we have mentioned above.

This was the first measurement we performed in the large series. Local defects and the quantifications of them, is left to the measurement of the single strip dark current, discussed below.

The set up is shown in figure 11. The probes touched the n^+ and the inner p^+ guard rings. We have also performed a test measurement polarizing to ground voltage both p^+ guard rings, beside, as usual, the n^+ one at the bias voltage. We didn't observe any relevant effect on the absolute value of the total current, while we have observed a slight decrease on the current of the border strips; this is discussed later. All the measurements performed using the p^+ guard ring, refer then to the inner one.

The detector is reverse biased by the *237* in the IV mode, with reading frequency of 32cycles/second and voltage scanning from +1volt to +70volt, giving an accuracy on the single measurement of the order of 0.01% and a sensitivity down to 0.1pA. Some typical curves for different detectors are superimposed in figure 12. One can see that the shape is substantially different from one detector to the other even taking into account the different depletion voltages. The sign of the I_T is positive since holes are collected at the p^+ guard ring.

Each curve can be interpreted as different manifestations of the current contributions. The relative importance of each single contribution varies very strongly from one detector to the other.

The I_g contribution is seen as a slow increase in the first part according to equation 4. A surface current effect can be seen in the

part where the curve is straight as a resistive behavior. A sudden rise at bias voltages much higher than the depletion voltages, is a typical indication of a breakdown or a first start of it in the junctions. Before that, there is an additional effect that most likely occurs [12]. The p^+ guard ring and the adjacent strips work as p^+np^+ junction [16]. When the crystal is overdepleted the p^+-n structure is reverse biased, while the other, the n-p^+, is forward biased. This gives a *punch through* or *reach through* current after full depletion is reached, with a sudden rise of the total current. The electrons go from the p^+ to the n, this is the leakage current contribution of each single strip seen at the guard ring. The holes are collected at the guard ring; their number suddenly increase when a small voltage over the depletion is added to drive forward the $n - p^+$ junction. To be noticed here that to be sensitive to this effect, the strips are left floating during the I_T measurement (figure 11). The *punch through* current [17] depends on several parameters of the detector: the strip-guard ring distance, the oxide charge, so its composition and quality, the voltage difference between strip and guard ring. It is therefore a good indication of the processing quality and it is used in the certification of the detector: section 4.3.2.

The quality certification is based on the I_T values at the voltages V_d and V_o, not on the shapes of the curves.

The homogeneity of the I_T values over the total series is discussed in section 5.2.3 as well as the quality criteria. To set these we have made the assumption that the I_T value measured can be interpreted as the sum of the contributions of the single strips dark current for which similar considerations on the relative contributions of the generation and the surface currents hold. It is therefore important to evaluate the single strip dark current; this is discussed in next section.

4.3.2 The single strip leakage current

These detectors can be readout using the interstrip charge division. The intermediate between two or more readout strips, are therefore as important as the bonded ones. It is then relevant to certify each strip and to disentangle the defects inherent to them.

To isolate the electric behavior of each single strip, we have used

the set up of figure 13. The bias and the probing were similar to the I_T measurement for the p^+ side but here we have probed also as many adjacent strips as possible, around the strips under test. This was possible, employing a probe card constructed on purpose (section 3.1).

The strip under test was sensed via the *237* in the IV mode by probing it with $+50mV$ and reading out the current (positive). The bias to the n^+ guard ring was supplied by the *230* voltage source, here used simply to keep the potential at constant V_o. The adjacent strips and the guard ring were constantly kept to 0V by the *595*. The number of strips biased was largely sufficient to neglect any contribution to the strip current due to the different potential of the remaining floating strips, except when defects were present.

A typical curve is shown in figure 14. The absolute value at depletion is very small (60pA). The shape is typical of generation-recombination current. This tells that all the effects external to the pure $n - p^+$ junction of the strip itself are negligible. In this situation, since the single strip current (I_{ss}), is very small, it is possible to disentangle even tiny effects of defective implantations, aluminizations, etching, of both the strip itself or the adjacent ones. This is possible thanks to the measurements with the probe card. For example if in the strip under test, etching was improper, it could cause the aluminum deposit to drop out of the implantation irregularly. Then a continuous metal path could be created between the jth strip under test (at positive +50mV with respect to the other adjacent ones and the guard ring) and, say the j^{th+1} strip which is at 0V. The resistance would be much lower than the interstrip resistance (section 4.5) between the two and the current of the jth strip would be very high with respect to the 0V level, which is of course the same for the measuring instruments, as described previously.

In the series measurements a scan over all the p^+ side strips was systematically done for all the detectors. The overall results are described in section 5. There we also illustrate the defects that this method allowed to detect.

In figure 15 we show the values of the I_{ss} for the p^+ side as a function of the strip number. It is clear that the value was pretty constant over many strips, typically 60pA, with a mean value of

150pA, and very few strips showing a current above 10nA. These values are excellent and they are used in the certification as quality criteria, described later. With an integration time around 1μsec of a typical VLSI preamplifier used in high energy physics experiment, the mean value current, of 150pA, corresponds to a 15enc as contribution to the input noise of the preamplifier, much lower than most VLSI preamplifiers which range around 300enc to 1000enc. This is also much lower than the noise due to the finite interstrip capacitance (section 4.4), of about 1000enc. In conclusion it is a very low noise contribution which allows to distinguish a most probable 24000e for a minimum ionising particle, orthogonally incident to the detector.

The strips in the vicinity of the guard ring were showing higher currents, closer they were to the edges. This is illustrated in figure 16. The mean value of the current is lower further we move to the center of detector. This behavior is expected, as there are less p^+ structures polarized in the vicinity of the strip under test. This is confirmed by two facts. The same measurement was performed with the addition of the polarization of the outer guard ring. The mean value of the I_{ss} was practically the same also for the strips at the edges or in most of the cases the difference was strongly reduced. The other observation which supports this fact is extracted by the scan plot (figure 15), in which a regular "gondola" shape is seen, both in the overall shape and in modulo 64. This is related to the way the measurements were done. In the scan, the strips under test at the very edges of the probe card, have only on the right or on the left side (in the case of the first and the last one, respectively) or have fewer strips polarized with respect to themselves. The innermost strip of each scan has the highest number of strips on its left and on its right that are adequately polarized, so it shows the lowest value. These differences are however relatively inessential, since the defects we have been looking for, manifest with order of magnitude differences, which is not the case here.

The n^+ strips showed a very different behavior in terms of leakage current. The measurement was performed in the single strip with the same circuitry as from figure 11. Here the p^+ guard ring was polarized to negative voltage and the current was sensed from the

n^+ strip via the *237*. In figure 17 the I_{ss} is plot. Since on the n^+ strips electrons are collected, the values of the current are negative. They are relatively high until "full depletion" is reached because in the n crystal the electrons are the majority carriers: their number is then drastically reduced at V_d. For higher bias voltages (i.e. in this case more negative, even if in the picture are indicated , for plotting purpose, the absolute values of the voltage), the current can be interpreted as a leakage current, corresponding to a reduced electrons flow as the free electrons are much less. This still tend to decrease. We believe that the main contribution to the remaining leakage current is, after full depletion, due to the flow between the p^+ implants in the same n^+ side and the n^+ strips. In particular the "u" shaped p^+ structures, which act as a reverse biased junction with the n crystal, contribute more to the reverse flowing of the holes, causing the flow of the electrons. The absolute values of figure 17 can be cross checked, knowing the interstrip resistance (section 4.5) and the voltage difference between the guard ring and the strip (section 4.6.2): for a voltage difference of the order of tenth of mvolt and an interstrip resistance of the order of few GOhm, the current is few hundreds pAmpere. This is an excellent behavior, given also the complexity of the implants in these region. This indicates that the fabrication process is well under control as illustrated more diffusely later for the large series results.

4.4 The interstrip capacitance

The measurement of the interstrip capacitance C_{ss} is relevant to evaluate the expected noise seen by each individual electronic channel when a detector is connected to readout electronics. As mentioned in the introduction, it is custom to connect the strips in the n side to the read out electronics via fan-out structure. These add up a linear capacitance to the input of the preamplifier. It is therefore relevant to measure the interstrip capacitance in particular for the n^+ strips. This is even more important in consideration of the fact that an aim of our test was to check the reliability of fabrication processes which were most delicate for the n^+ side.

The interstrip capacitance depends on the geometry of the strips, the length and the width of both the implantation and the alumin-

isation. A dependence on the depth of the implantation reflects rather on the measurements response than on the intrinsic capacitance characteristic.

The set up for the measurements on the p^+ strips, is illustrated in figure 18; for the n^+ side, it is symmetric.

We show the curves for the p^+ and n^+ side (of two different detectors) in figure 19 and 20 respectively. The fact that it is not constant after full depletion, is due to the influence of the adjacent p^+ implants. The phenomenon is very much similar to what we have discussed in section 4.3.1. At their edges the p^+-n^+ structures are slightly different among each other and they tend to deplete at different voltages. In the curve it can be seen the effect of different junctions or portions of a junction [18]. However the values on many strips concentrate in a small spread interval. The C_{ss} wasn't a parameter used for the quality certification, in the strict sense of tagging a detector as *"working"* versus *"malfunctioning"*. We therefore report simply the cumulative results in section 5.

Figure 21 shows that the C_{ss} measurements cluster all around the same value, with a mean of 7.465pF for the p^+ strips and 9.453pF for the n^+; this gives 1.060pF/cm and 2.716pF/cm respectively. For comparison the value for the n^+ strips must be divided by 2 since the aluminised pitch is twice than for the p^+ side. This ends up to a mean value of $\approx$ 1.220pF/cm, typical for high resistivity silicon.

According to the equation 3, where the thickness of the wafer must be now substituted by the interstrip pitch, the C_{ss} mean value can be used to calculate the depth of the depletions region at the implantations active in the capacitive coupling. Before doing that, we verify the consistency of the C_{ss} values obtained, by taking the ratio to the capacitance to the back plane for the single strip under measure: we call it C_{sb}. This is slightly different from C_b, the bulk capacitance described in section 4.2. From literature, we have [19]:

$$\frac{C_{sb}}{C_{ss}} = \frac{ln(\delta/w)}{ln(4t_d^2/w\delta)} \tag{5}$$

with

δ, aluminised strip pitch;

w, strip aluminisation width;

t_d, depletion thickness.
For the p^+ side:
$\delta = 25\mu\text{m}, w = 12\mu\text{m}$.
For the n^+ side:
$\delta = 50\mu\text{m}, w = 12\mu\text{m}$.

Equation 5 holds strictly speaking for the interstrip capacitance of one strip with respect to the first neighbor, neglecting the effect of the next ones.

This doesn't allow to evaluate the difference in the depletion voltage and depth seen by the single strip, from the one measured with the test diode [20], but we can cross check the measured C_{ss} values, using the ratio of equation 5.

Taking the value of $t_d = 277\mu m$ and correspondingly $C_b = 3.560pF$, we find:

$$\frac{C_{sb}}{C_{ss}} \cong \frac{C_b}{C_{ss}} = 0.092$$

and for $t_d = 315\mu m$ and correspondingly $C_b = 3.1pF$:

$$\frac{C_{sb}}{C_{ss}} \cong \frac{C_b}{C_{ss}} = 0.093$$

Comparing the two values, respectively for

$$t_d = 277\mu m \qquad \frac{C_{sb}}{C_{ss}} = 0.106 \tag{6}$$

$$t_d = 315\mu m \qquad \frac{C_{sb}}{C_{ss}} = 0.102 \tag{7}$$

we see they are within expectations.

4.5 The interstrip resistance

The final use of these sensors is potentially always for charge partition read out. The charge sharing between strips must therefore be

possible. The interstrip resistance R_{ss} can't then be too high (not $\gg 10\text{G}\Omega$). On the other hand the processing of the n^+ side doesn't allow to reach very high values, since the the interstrip resistance is essentially due to the p^+ blocking implantations, in between the strips. The processing specifications and the geometric constraints for the implantations are such that the interstrip resistance is not higher than $10\text{M}\Omega$.

The principle of the measurement of R_{ss} is schematically illustrated in figure 22 for the case of the p^+ side. The voltage difference applied to the adjacent strips is low (between $-250mV, +250mV$) with respect to the bias voltage, in order not to perturb the biasing and not to damage the implantations, but enough to exploit the measurement.

For the p^+ side, the values measured are only an upper limit. Infact the resistance of the coaxial cables we have used, is (as it is typically the case) of the order of a $\text{G}\Omega$. In the circuit, this is the resistance to ground, or better, the equivalent one of all the resistances to the opposite polarized strip, which in turn is at the ground potential. Then if the resistance of the cable dielectric, to ground, is lower or comparable with the interstrip resistance, then the current will flow also or only to the cable dielectric and not in the interstrip zone.

Much more sensitive is the measurement on the n^+ side. In this case the bias voltage was applied in the p^+ side and of reverse sign. As it is clearly seen in figure 23, the resistance is very low until full depletion is reached. Then at values of the bias voltage very close to depletion, the curve shows a sudden rise, due to the fact that most of the free charge of the crystal have gone away. For bias voltage higher than that, the curve should have a constant slope of $\approx 2,5 \cdot 10^{-3}\text{volt}/50 \cdot 10^{-12}\text{A} = 50 \cdot 10^6\Omega$. This is the slope which is evident in figure 25. However, after V_d, the increase of the current is not exactly linear. This is due to residual charge in the junction between the n^+ and the p^+, which, with increasing voltage, is carried away.

This is relatively important: the value measured at V_d, is anyway already very good to exploit the detector in charge sharing readout, also for the n^+ side.

4.6 The voltage difference between guard rings and strips

Since these are double sided sensors, there is a choice as in which side to put the bias voltage, as well as the sign of the polarization of the guard rings. Beside the common use of the guard ring as a blocking implantation to limit the surface leakage current, for this detector there is also the possibility to profit of its polarization, to bias the whole detector and to optimize its performance.

This is done in both sides, by tuning the distances between the strips and the guard ring, in the fabrication processes and then polarizing the structures adequately as described below. In addition in the n^+ side the p^+ implantations themselves are used to define the voltage of the whole side.

4.6.1 The punch through voltage in the p^+ side

To operate the detector, at the p side guard ring, a positive voltage is applied to bring all the p^+ strips to the same potential and avoid excessive unbalancing with respect to the front end electronics. In this way one makes use of the punch through effect in between the p^+ implants of each strip and the p^+ implant of the guard ring, being both embedded into the n type crystal [16] , [17]. As a current punches through, one can measure the equivalent voltage drop (see the set up of figure 24). For example, if the detector is biased and if the guard ring (or viceversa the strips) were left floating with respect to the strips (or viceversa the guard ring), typical values are of the order of few volts. When operating the detector one therefore has to compensate by this amount to better equalize the potential, then the response, of all the strips. A typical measurement of this quantity is reported in figure 25 where the current applied in the guard ring was positive, as well as the bias voltage in the opposite side: the measured voltage (of the same sign) shows a logarithmic behavior after depletion is reached. One therefore can choose a certain voltage value after depletion is reached in the region after the bending of the curve. This will be the absolute value of the polarization voltage of the guard ring when running the detector. Its sign will be positive as one has to compensate by this drop. At this value there is therefore a fairly good stability and, more

important, a fair homogeneity between the strips.

4.6.2 The voltage drop in the n^+ side

At the n^+ side the implants of the p^+ blocking strips have "u" shape at the edges, of $500\mu m$ length (section 2). They act as resistors to the current flow when the detector is reverse biased. The distance between the extremity of them and the guard ring is 5μm. The voltage drop from the guard ring to the edges of the n^+ strips is therefore due to the current flowing through the n crystal and through the surface over these distances. Given the measured interstrip resistance of the order of $\approx$MΩ (section 4.5) and the single strip current of the order of $\approx$pA, then the voltage drop on this side is only of the order of 10^{-3}V. To calculate the expected voltage difference between the guard ring and the n^+ strips, one has to evaluate the effective resistance to the current flow, due to the presence of the p^+ implantations and disentangle the surface to the bulk contribution. This is not possible as it was not for the interstrip resistance. Furthermore in the measurement of the interstrip resistance, the contribution of the resistance to the guard rings, was included, since it is not possible to disentangle the surface leakage current contributions, neither due to the flow towards the guard rings, nor towards the adjacent strips. It is however intuitive to estimate the contributions as half due to the guard rings current contributions and half due to the leakage through the adjacent strips. Although the length of the "u" terminations is much smaller than the length of a strip, they contribute by twice the same amount.

In conclusion the expected voltage drop in the n^+ side is of the order of mvolt. This can be seen in figure 26, where the measurement performed with the set up similar to figure 24, is reported.

5 The tests on a large series

Here we describe the experience on testing a large number of double sided detectors. The production started after a pre-series prototype check and it has continued in parallel with the testing. This allowed us to bring immediate feedback for subsequent series to the

manufacturer, to improve with time the acceptance rate and the understanding of the failures. This procedure involves the manufacturer more directly, a fact which also contributes to improve the confidence on the technology. We demonstrate it is also more efficient, both in terms of manpower and money, showing a failure rate rapidly decreasing with time and with the number of tested detectors.

Beside the failure rate, another parameter, we could control, was the efficiency versus time. We were able to finalize rapidly the testing procedure, to disentangle the weakest fabrication points and monitor them continuously, all within a strict fabrication and testing schedule. We have optimized the tests to have a first general knowledge of the quality of each detector, then deciding how to proceed for further diagnostics. In the following we describe the operations undertaken and the relative time spent on each of them, during a typical detector test.

5.1 The serial operations

The strict schedule and the experience on the first prototype, guided us for the definition of the testing steps listed below. Some of them may look trivial, but one has to keep in mind that any mechanical and optical operation is on a μm scale, so to suppress the possibility of making unrecoverable mistakes, we had to act with great care and relatively slowly. Therefore each step, even the simplest one, was quite time consuming and we had to take it into account when running over the entire series, to account for the total time spent per each detector. We list here all the operations we have regularly performed.

- [i] Visual inspections (naked eye and microscope) after dry air cleaning or eventually acetone with a soft cloth was used if unusual spots were apparent.
- [ii] Mounting of the testing diode on the jig and then inside (needles positioning) the probe station for the measurement of the *depletion voltage* V_d and the *operation voltage* V_o.
- [iii] Run for the CV curve, determination of the knee via the linear fit, annotation.

- [iv] Dismounting of the diode.These first four steps were repeated for the all batch, before proceeding to the next ones, to save time on mounting the diodes on the jig and on switching the running acquisition.
- [v] Mounting of the detector with the p^+ side up on the jig and then inside (needles positioning) the probe station, for the *total current* I_T measurement.
- [vi] Run the IV acquisition for the I_T curve, determination of the values corresponding to V_d and V_o, annotation.
- [vii] Positioning of the probe card needles for the I_{ss} measurement.
- [viii] Run for the I_{ss} curve; this measurement is done in steps for each 56 strips to probe all the p^+ strips, then the strips indicating abnormal values were noted; these last two operations (vii and viii) were repeated seven times.
- [ix] Positioning of the needles for the voltage drop measurement.
- [x] Run the VI acquisition for the voltage drop curve, determination of the values corresponding to V_d and $2\times V_d$, annotation.
- [xi] Dismounting of the detector, storing.

  All the operations described above were repeated for all the detectors for all the batches. In the following are listed the measurements performed only in sample of detectors for each batch, since the experience indicated that this was far enough for suitable monitoring of the fabrication.
- [xii] Mounting of the detector with the n^+ side up on the jig and on the test station.
- [xiii] Positioning of the probe card needles for the I_{ss}.
- [xiv] Run the IV measurement for the I_{ss} curve; this is done in steps for each 56 strips to probe all the n^+ strips, then the strips indicating abnormal values were noted.

The operations [xiii] and [xiv] were then repeated 15 times.

The time spent for steps [i] to [iv] was around 30min per wafer; for steps [v] to [xi] 180min per detector. Overall we have observed that, in average, and "at regime", we needed 4hours per detector.

All the measurements listed above were the most time consuming and they were regularly performed.

We performed additional measurements to monitor the interstrip resistance and capacitance on both sides, even if drastic variations were not expected neither measured (see section 4.4 and 5.2.6).

5.2 The cumulative results

In the following we describe the results on the total series of 255 detectors, namely on the quantities used for quality selections. We have also set the acceptance limits for the total leakage current and the single strip leakage current.

In section 5.2.8 we summarize the acceptance rates.

On the guard ring - strips voltage drop at the p^+side and on the interstrip resistance resistance on the p^+ side, we have performed systematic checks measurements as well, with the aim of monitoring the production but no acceptance threshold was set. This was possible thanks to the fact that all the detectors which passed the previous leakage current tests, had all a fair value for the voltage drop and the interstrip resistance. For these quantities we report results only for a subsample of the detectors.

5.2.1 The sample

The results concern a large sample of 288 detectors produced and serially tested in about 320 days. This includes also the time to produce the first prototype batch and to test it more extensively, halting the production for few weeks. All the accidents time is included on this total, even if these were minimal on the production (occasionally due to installation faults, independent from the operators actions) and practically none on the testing. The total time includes as well the delivery time, which, given the delicate material, the large quantity and the continuous output from the company, deserved a special care for optimization and safe operation.

5.2.2 The results on the depletion voltage

The wafers used were coming from different production lots of the same company; we therefore expected a variation in a relatively large range of resistivity values, i.e. in the depletion voltages. It is relevant to monitor this variation since it reflects on the operation voltages to set when the detectors are mounted on complex structure, this requiring adequate pairing of the wafers, on the basis of their depletion voltage. This is practically possible only if a safe operation voltage interval has been defined.

To show that we had a comfortable spread of the minimum and maximum allowed voltages, as an interval of safe operation for bias voltage on all the tested wafers, we report in figure 27 the range of variation. There it is shown (for about all the tested detectors, namely 191 units) the minimum voltage at which each detector was safely depleted (equivalent to the value just above the knee in the CV curve, see figure 8) and correspondingly the maximum voltage (full dots) value, above which the curve of the total current (I_T) has a steep increase. Empty dots show the minimum voltage below which the corresponding bulk capacitance (C_b) values are no longer constant.

It is remarkable the result that the bias voltages can be set in a wide interval, to operate any of the detectors in overdepletion, when paired with any one of the others.

5.2.3 The results on the total leakage current

The value of the total current I_T was used to select the quality of the detectors. A detector showing a I_T much larger than the sum of the single tolerable single strip leakage current (see 4.3.1), when biased at V_d and/or at V_o was discarded. Summing up a typical value of 60pA over 1500 strips of the p^+ side, this amounts to 90nA. Even if one takes the mean value of $I_{ss} \cong 150pA$, this gives 0,25μA. We set a safe threshold value of $I_T = 2\mu$A at V_o. In figure 28 we show a distribution of I_T for more than 200 detectors. The discarded detectors are at high values of leakage current indicating that the threshold value was safely set. This was considered as an independent selection cut, sufficient to discard a detector. In this

way only a small percentage of detectors were discarded, namely the 11% of the total. This, together with the other failure rates, will be rediscussed in the section 5.2.8. We are convinced that most of the faults can be detected via this measurement, even the most hidden ones, like bulk defects, macro cracks in the crystal, excess of surface charge.

In most of the cases, a detailed analysis of the cause of this failure was not done. Not all the detectors which passed the I_T selection criteria, were accepted. A detailed analysis of the faulty cases was performed if the detectors showed anomalous behavior in one of the measurements described below, after passing the I_T selection cut.

5.2.4 The results on the single strip leakage current

The measurement of the single strip leakage current I_{ss} is crucial to have a detailed information on the behavior of each single implantation.

The typical or the mean single strip leakage current was measured on the p^+ side for each detector and for every strip, while on the n^+ side sampling for every batch one detector. We found that the I_{ss} on the n^+ side did not depend on the production batch, unless specific faults of the production were present in a particular batch. These cases are described in section 5.2.7.

We plot in figure 29 the distribution of the mean of the I_{ss} values on the p^+ side, for several detectors on all the batches. From that one can infer the typical value of 60pA and the mean of 150pA for the I_{ss} on the p^+ side.

As discussed in section 4.3.2, the value of I_{ss} of 150pA is already a good guarantee of correct behavior of the strip. To define a selection criteria of rejecting a detector, we first recall that a current of 50nA, fairly higher than the typical and the mean I_{ss}, still gives a very low noise contribution, both with respect to the interstrip capacitance and to the input noise of a preamplifier. We then set a safe limit value of 50nA to tag a strip as malfunctioning. This value is, actually, very rare as it can be seen in figure 29 and it corresponds to a low additional noise contribution to the input of the preamplifier, of about 500enc.

The equivalent noise charge due to dark current, influences the

global performance of a detector, used in high energy physics experiments. To identify a cluster of charge due to a particle, one has to set a threshold above the noise, which is usually defined as the r.m.s. of the pedestals after common noise subtraction, for many events and many channels. Depending on the number of the channels used, one or more malfunctioning strips, will influence the calculation of the r.m.s., so at the end the definition of the cluster charge. This will not produce fake hits in a detector, but rather, will produce dead zones. We decided to accept detectors having at most 2 strips with more than 50nA current. This should keep at the level of 1% the dead regions, even assuming all the wafers in a detector have these defects.

On a total of 255 detectors, we have found 23 with more than 2 malfunctioning strips. In figure 30 we show the distribution of the number of detectors with one or more strip with I_{ss} higher than 50nA. The entries left out of the plot are only 12. In total this gives 158 detectors. Taking from the plot the number of strips/detector, this gives 863 strips over a total of $1500\text{strips} \times 255\text{detectors} = 382500\text{strips}$ i.e. only 0.2%. We also have included in the plot the bin of non defective strips of the p^+ side for all the detectors. It is clear that the quality cut we set is very safe, although discriminating all the defective detectors. We went into deeper analysis of the defects for these detectors. This was possible because we localized the defects identifying the malfunctioning strips. Indeed, we found that most of the times the faults were caused by a specific unsuitable processing. In most of the cases infact we found the defects very much localized in more than 2 strips, for a region of several strips, showing values of I_{ss} much higher than the acceptance threshold of 50nA. We found that there was a current path between adjacent strips. The reasons, the failure rate and the cures of this defect are described in section 5.2.7 and 5.2.8.

5.2.5 The results on the voltage drops

We have measured the voltage drop between guard ring and strip on the p^+ side. for all the detectors which passed the total leakage current selection even if not satisfying the I_{ss} cut. We have done this in order to monitor a different phase of the production, which

influences the gap between the guard ring and the strips. All the measured values indicate that all the detectors satisfied the specifications for production. In figure 31 we show the distribution of the voltage drop in the p^+ side measured at the depletion voltage and at twice the depletion voltage. This implies that a safe interval of operation was possible for all the selected detectors, not only for pairing on the basis of the operation voltage (see section 5.2.2), but also on the basis of the voltage drop.

5.2.6 The results on the interstrip resistance

The interstrip resistance was measured only on a limited number of detectors of the large series. We started by measuring on a pair of strips of the p^+ side and n^+ side, on each detectors of the first few batches. Given the very homogeneous values obtained, we decided to sample only one detector per batch. Since the measurements on the voltage drop gave also an indirect indication also of the interstrip resistance on the p^+ side, we then sampled n^+ side strips, most delicate on the processing (see the discussion in section 4.5). Figure 32 shows the distribution of the values measured for one pair of n^+ strips in different detectors. Although the number of detectors is limited, it is evident from the distributions that the detectors were all very homogeneous on the interstrip resistance values, as stated above.

The plot of the values per different pairs of strips but on the same detectors gives similar results as in figure 32.

5.2.7 The failures and the cures

In this field we very often observe rapid and frequent development. This leads to assiduous interactions with the fabrication companies. Given the development aspects, it is often quite difficult to disentangle between the failure on the prototypes and the large, equal to themselves, series of the very same objects (chips, detectors etc....) [21]. The case we have discussed here, is in between and it constitutes an example on how an under development process goes with success to series regular production. The failure cases we present here are therefore to be considered as further acquired

knowledge for the large series processing and not prototype results. This gives higher confidence on the fabrication processes and it has been achieved (and in our opinion it can only be) thanks to the cooperative efforts of the company.

As mentioned in section 5.2.4, the most frequent failure we have observed, was a short, low resistance, current path between adjacent strips. After detecting a very high value of I_{ss}, ranging from 500nA to few tenth of μA, in one or more adjacent strip, we checked by microscope and we found large unequal spots of aluminum on a small region covering the high current strips (figure 33). We could ascribe that to improper regular cleaning of the mask, during the fabrication process. After photoetching, the detector masks were washed by immersion in a bath for the removal of all deposits. The cleaning was regularly done but the occurrence of the defects demonstrated that it was sometimes not sufficient to remove completely all the deposits out of the mask. The reason for that was difficult to identify, but a longer bath time helped to avoid in subsequent batches, most of the defects.

As we have mentioned earlier, we could regularly test the detectors per production batch, so we could detect this defect only after a full batch was completed. The defective region was most of the times of the order of few millimeters, of the same brilliance of the strips, being aluminum, so it was impossible to identify it by the regular naked eye or microscope inspections.

In figure 34, we show a plot for several detectors which belongs to one of these batches. We plot the number of times a strip has given an high current value (see section 5.2.4 for the values), versus the strip ordinal number on the p^+ side. Thanks to that plot, we could identify the localized defects in a precise portion of the mask. We found out that some material was left attached to the mask for subsequent exposures, in a well identified region, corresponding to the faulty strips.

The deposit defects were present on a large part of a full batch and the following one of the same pair[10]. We adopted a more frequent and longer time of the cleaning of the mask, but this, although

[10]we remind that in the production line two batches always arrived together with a time shift of one week

it could eliminate the defect on most of the following batches, it didn't cure it completely. We decided then to make microscope inspections of the detectors, at the company and to remove the eventual excess of aluminum by tungsten micro-needles. This procedure turned out to be very successful and allowed us to rescue near the total of the defective strips (typically 85% of them and/or of the detectors). To illustrate that, we plot in figure 35 the number of strips, for trial batch, with defects, before and after intervention, for several detectors. Most of the times, the intervention removed the defect, leaving only one strip with high current, as we verified with additional tests. Given our acceptance criteria (section 5.2.4), we could then include these detectors in the accepted categories. Since in the following batches we encountered much lower number of these defects, these additional cures and checks didn't substantially increase the series testing time.

The one described above was the most striking example of a failure and a cure process. At the very beginning, in the very first batch, we had experienced very large total leakage current and very low voltage drop values on the p^+ side, due to missalignment of the mask by only few microns. After realigning the system this had never shown up again. At the same time for the very first few batches, we had experienced some rare mechanical defects, detected by large total leakage current, due to crack of the crystal. More care on handling in all the phases after the production up to the test, together with very fine tuning of the dicing parameters at the cutting phases at the same company, almost removed these events. The incidence of all these cases on the total failure rate are described in next section.

5.2.8 The failure rates

Here we collect all the results reported separately in the current section and we put them together to quantify the influence of each of the failure causes.

The acceptance rates are shown as function of batch number. We remind that the ordinal number of the batch follows the fabrication time, i.e. lower is the batch number older is the fabrication date. One can see the improvement with time and the essential role played

by the serialization of the tests described here. In figure 36 we show the overall rejection rate on the basis of the total leakage current. On a total of 255 detectors, only 28 were not accepted for high total leakage current, which gives a rate of $(11 \pm 6)\%$. In addition the differential rejection rate decreased steeply also in percentage per each batch, as indicated in the curve of figure 36.

Figure 37 shows the overall rejection rate on the basis of the single strip leakage current. On a total of 255 detectors, only 23 were not accepted due to high single strip leakage current for more than 2 strips. This gives a rejection rate of $(9 \pm 6)\%$. We remind that the detectors, failing because of the aluminum deposition defect described in the previous section, are counted here if they still do not satisfy the acceptance criteria of section 5.2.4 even after the repairing intervention. Therefore, in particular thanks to the curing of these failures, the differential acceptance rate on I_{ss}, increased steeply as function of batch number. This is shown by the dashed curve of figure 37.

We have mentioned that the leakage current has been by far the most decisive parameter for the quality selection of the detectors. We however had a very small number of detectors, out of the production line, which could not be used because of miscellaneous reasons, almost all due to mechanical defects. These are indicated in figure 38 where we report the number of detectors accepted out of the production together with the ones rejected for the three causes described above.

To give an important evaluation also of the effectiveness of the production we have compared the number of wafers commissioned to the various companies in the different phases versus the number of detectors actually produced. This includes then three different companies for the three basic processes described in section 2: the wafers production, the wafers polishing, the detectors fabrication on the wafers and the detectors cutting out of the wafers. This last in particular we have included in the detector fabrication as it was very well done at the fabrication company, although not essential. Figure 39 shows the number of wafers or detectors out of each of the three steps, compared to the ones commissioned to each company. The last bin gives the total number of detectors accepted to be compared

to all the wafers commissioned at the beginning.

We believe that the cost of large scale detectors is a very relevant parameter, however a comparison is not done here, as this is rather elusive subject, depending on many variables, like the raw material delivery, the fabrication places and others. We simply report the comparison of commissioned versus accepted ones, to give a rough idea of what one can expect going from the first orders down to the finished fully functioning detector.

6 CONCLUSION

For the sake of the subject of this paper, we concentrate on the total number of detectors which were produced and the ones which passed the selection criteria. This is illustrated in figure 40. The overall excellent acceptance rate of $(78 \pm 5)\%$ is not simply due to very high quality processing. On the contrary we claim this was due to the very fast and reliable feedback given to the fabrication lines, thanks to the large series testing procedures and set up described here. This improved clearly the fabrication processes, in terms of speed and reliability, thanks to the detection of even tiny processing defects.

We have demonstrated for the first time that large series production and testing of double sided detectors are feasible in relatively short time with very high quality requirements. For that it is mandatory a very close interaction with the fabrication company.

It is therefore possible to undergo construction of very large high precision detectors for medicine, space or nuclear and high energy physics application, based on double sided silicon microstrip detectors.

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Table I Detector dimensions (μm)

quantity	p strips side I	n strips side II
length	70400	38400
number	1536	1408
pads	200×50	200×50
pitch	25	50
width	10	10
thickness	1	1
Al pitch	25	50
Al width	12	12
Al thickness	0.5	0.5
g. ring pitch	10	
g. ring width	100	500
detector sides	72000	42000

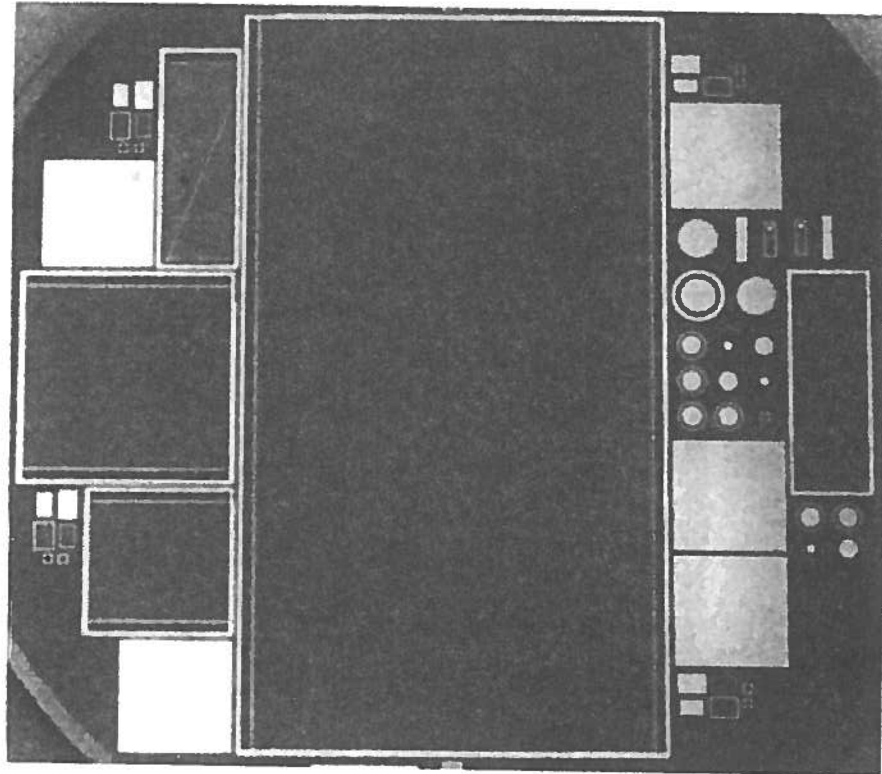


Fig.1 Picture of the wafer after processing; the detector is the central rectangle, some of the test structures are visible.

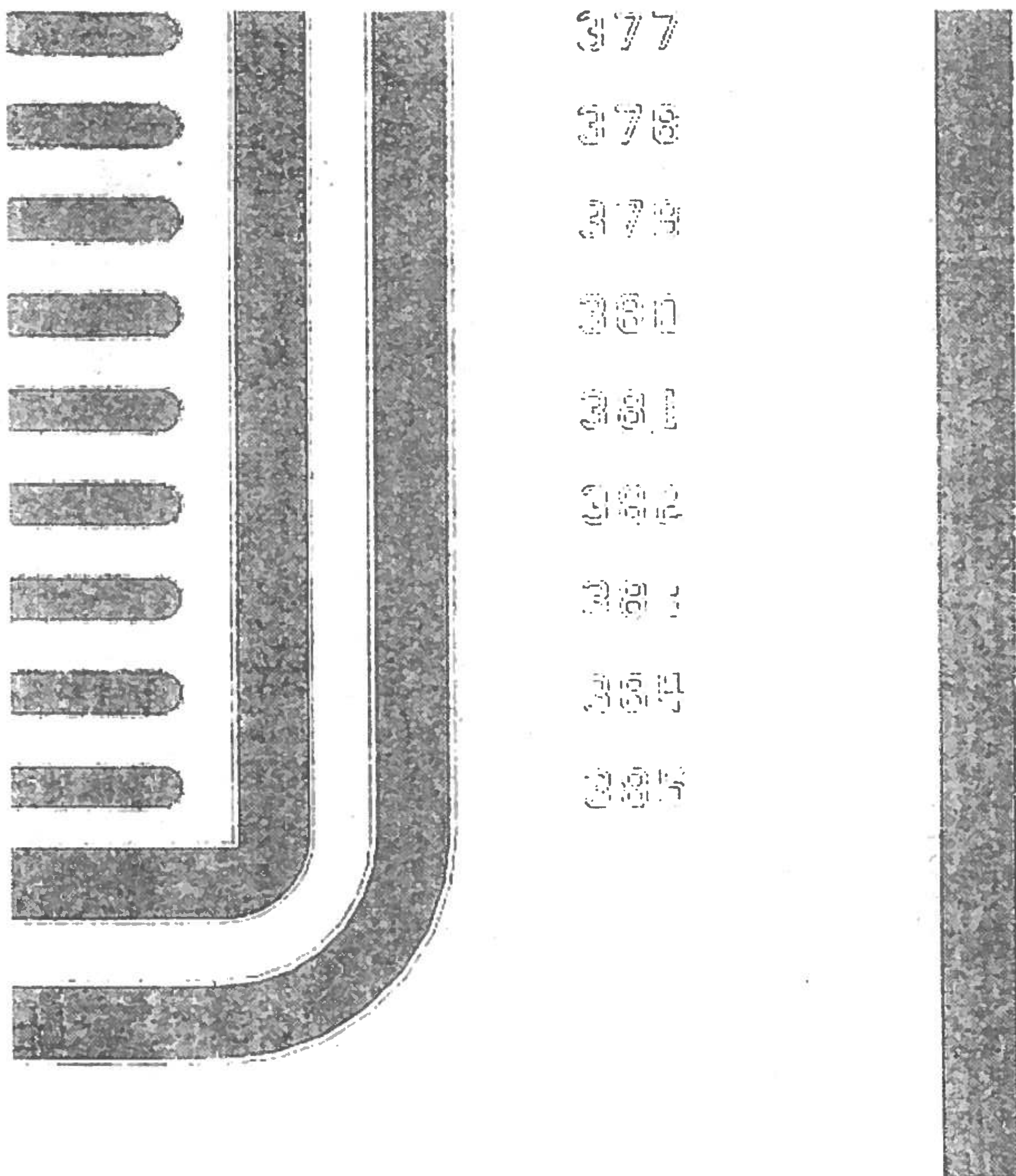


Fig.2 Sketch of a detail of the mask in the p^+ side.

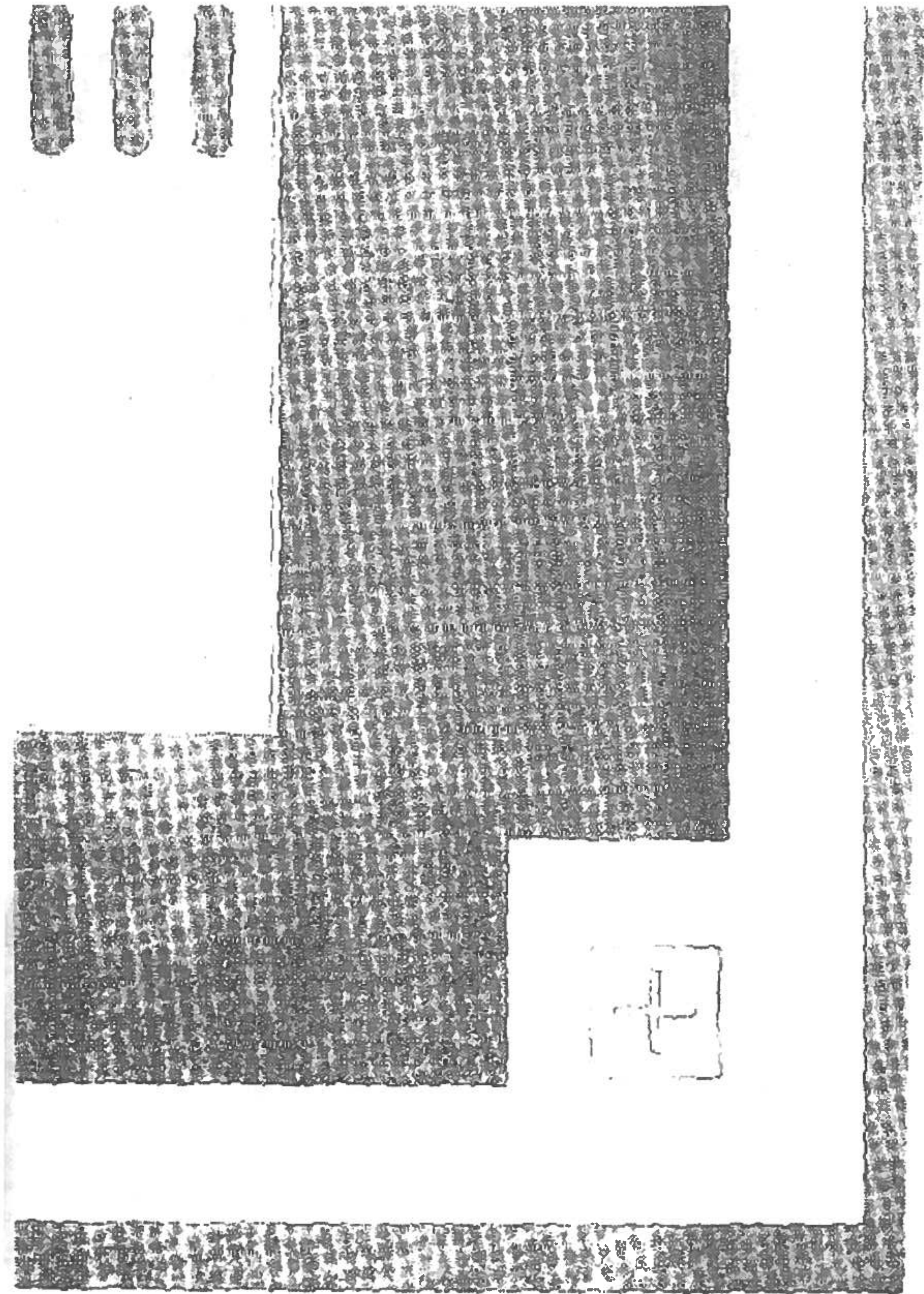


Fig.3 Sketch of a detail of the mask in the n^+ side.

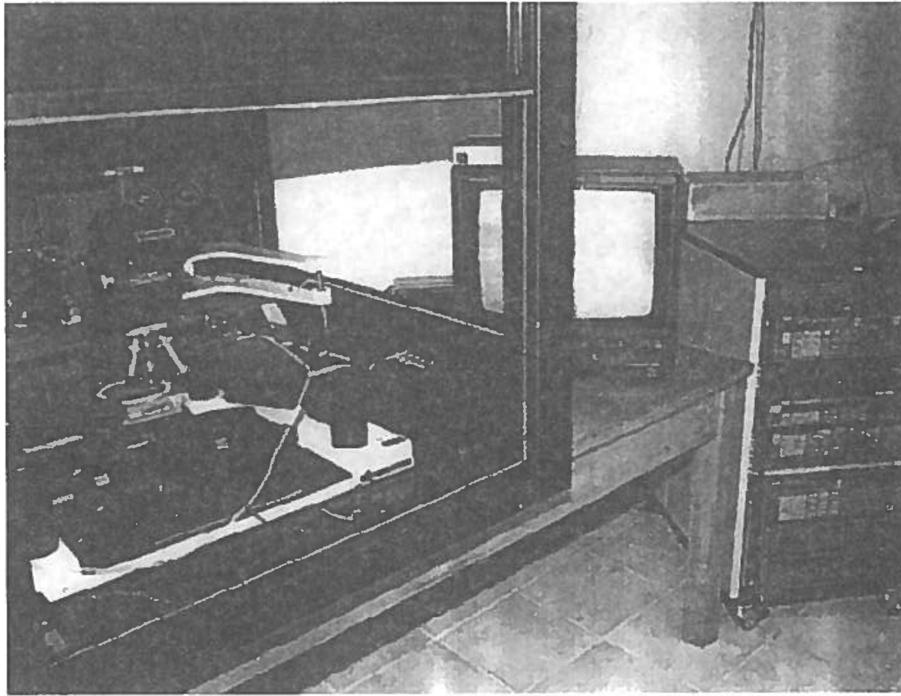


Fig.4 Picture of the test station and the set up; the probes and a detector mounted on its jigs are visible.

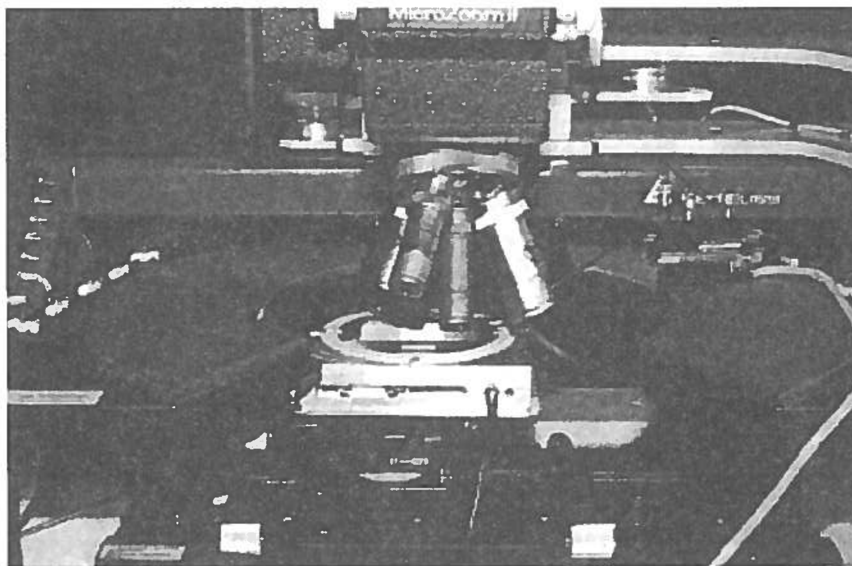


Fig.5 Detail of the detector mounted on the jig; it is visible the n^+ side, with the probe needle for the bias in this case on the backplane.

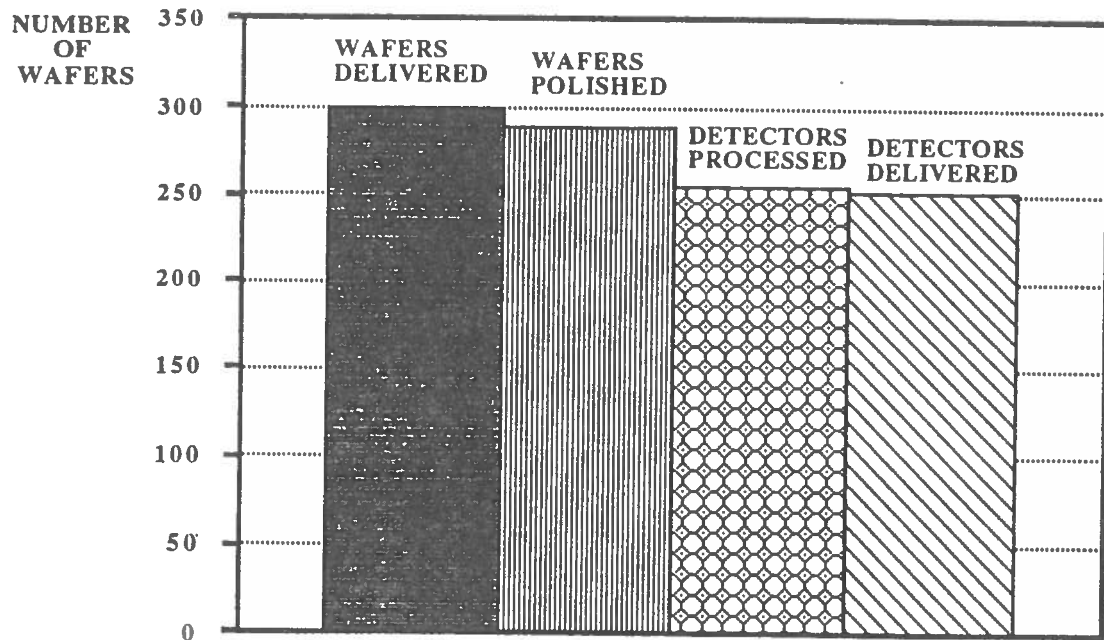


Fig.6 Number of detectors before and after the single operations.

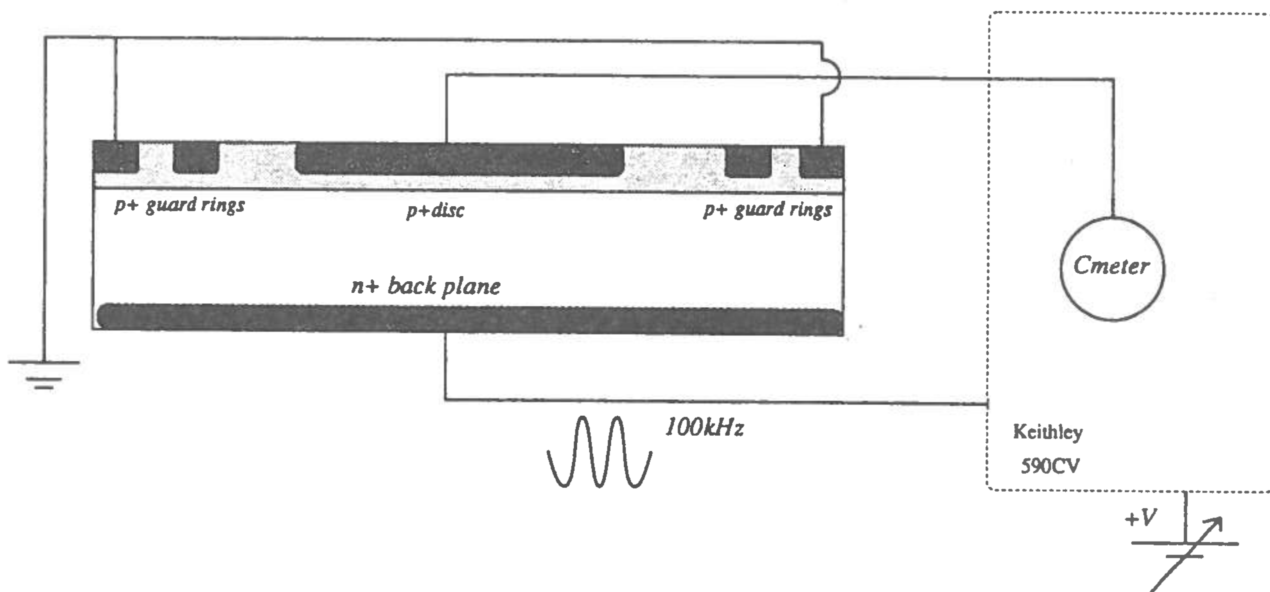
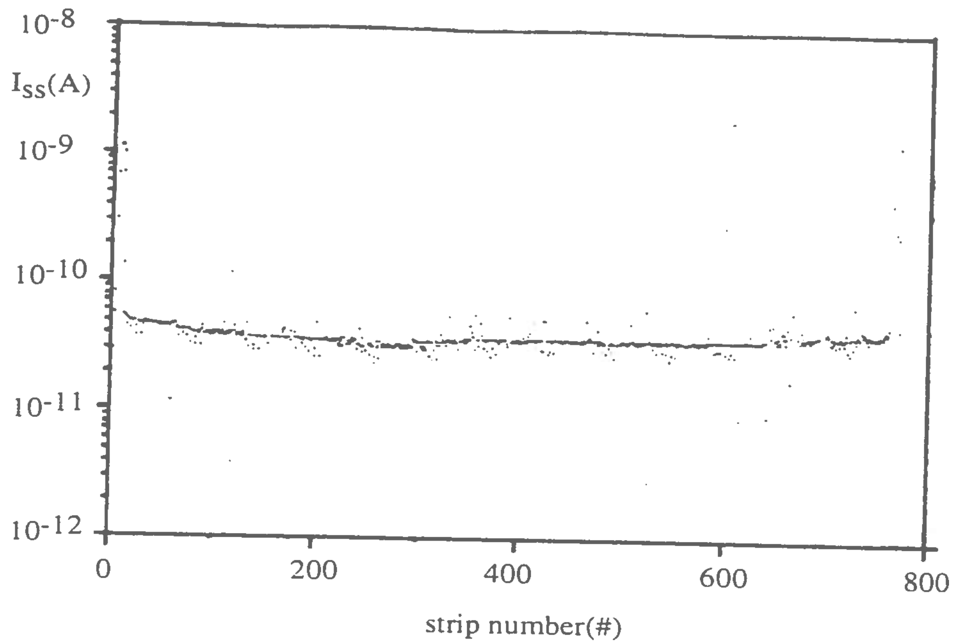


Fig.7 Set up for the C_b measurement.



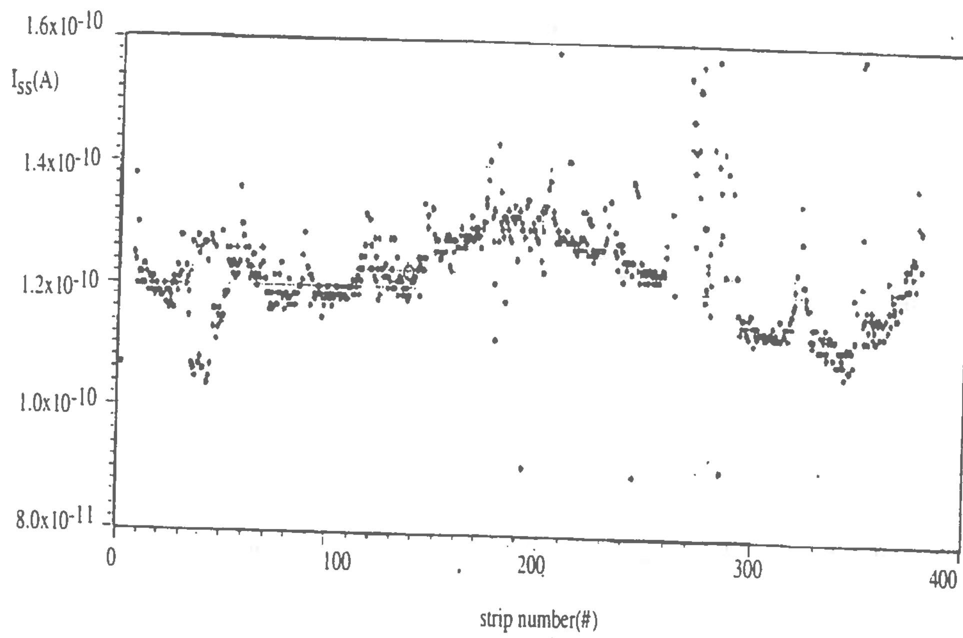


Fig.15 Scan of the I_{ss} values for all the p^+ strips for two different detectors; scales are different.

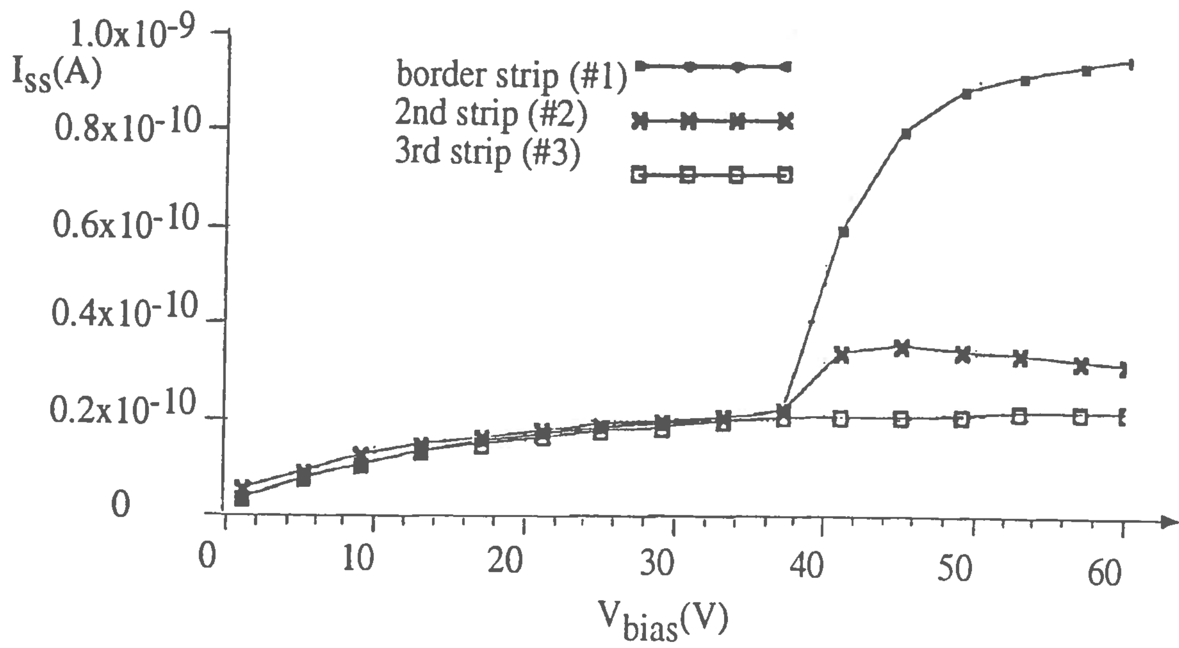


Fig.16 Typical I_{ss} curves for 3 p^+ strips closer to the guard ring.

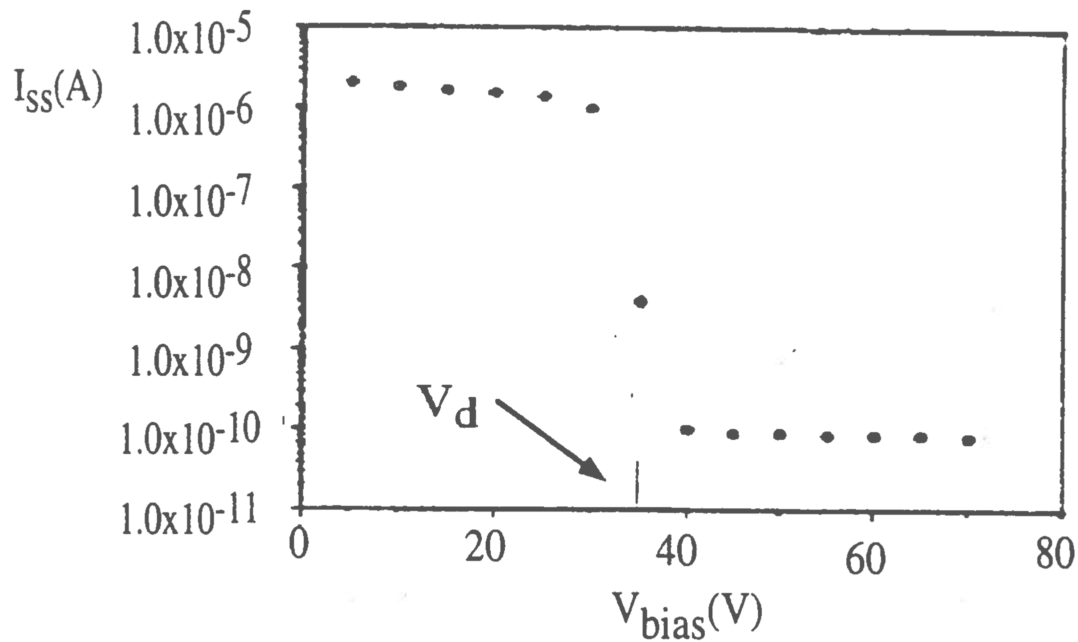


Fig.17 Typical I_{ss} curve for a n^+ strip.

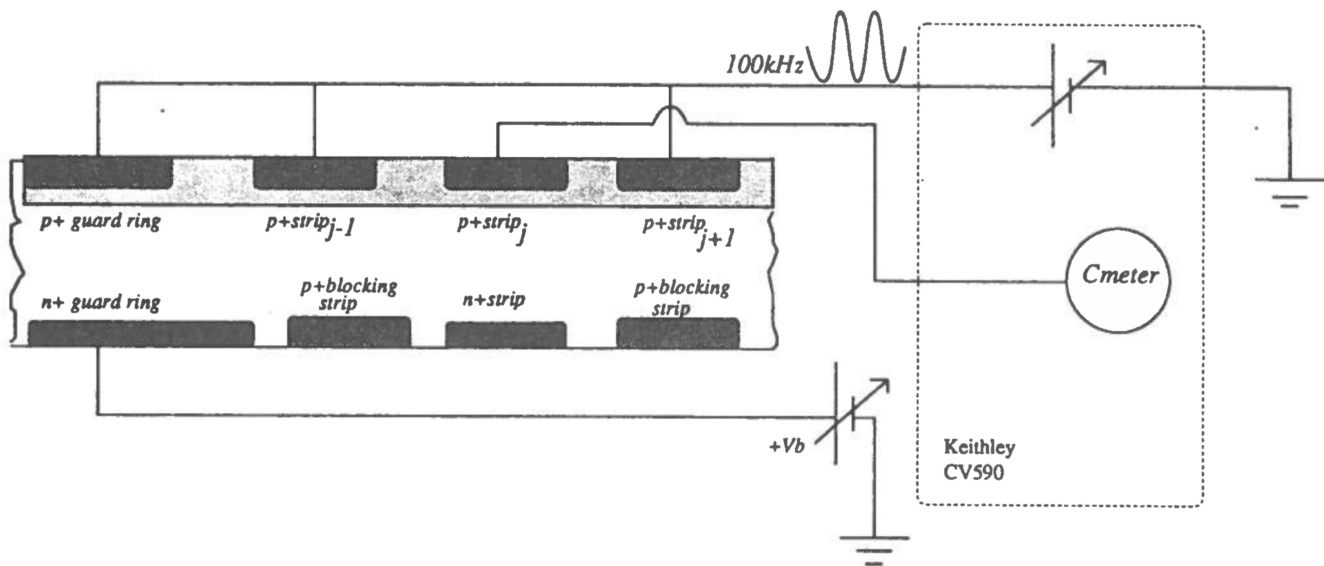


Fig.18 Set up for measuring the C_{ss} curve for the p^+ and n^+ side; here it is schematically illustrated the case for the p^+ strips.

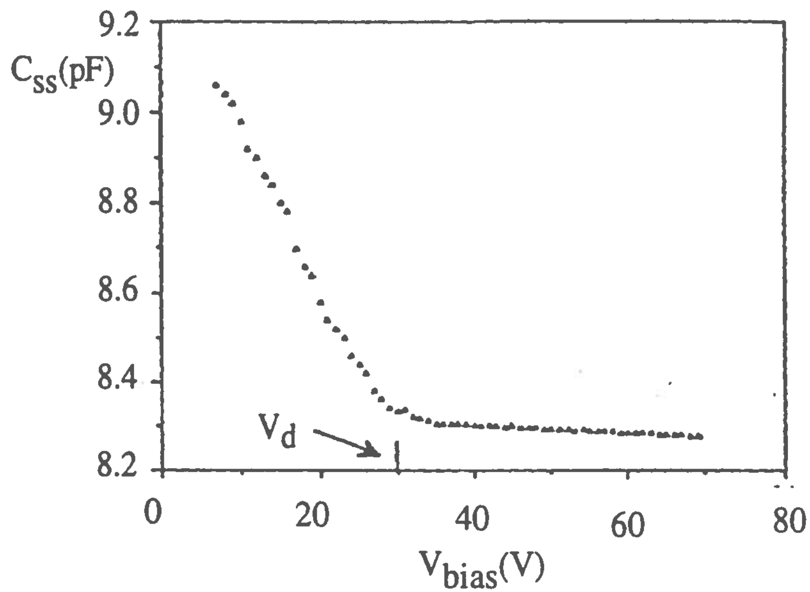


Fig.19 C_{ss} curve for the p^+ side.

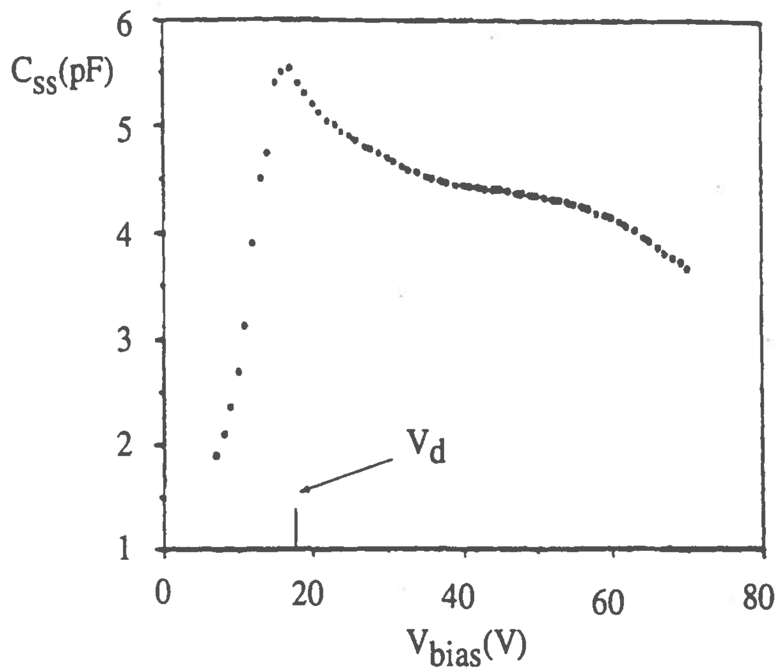


Fig.20 C_{ss} curve for the n^+ side.

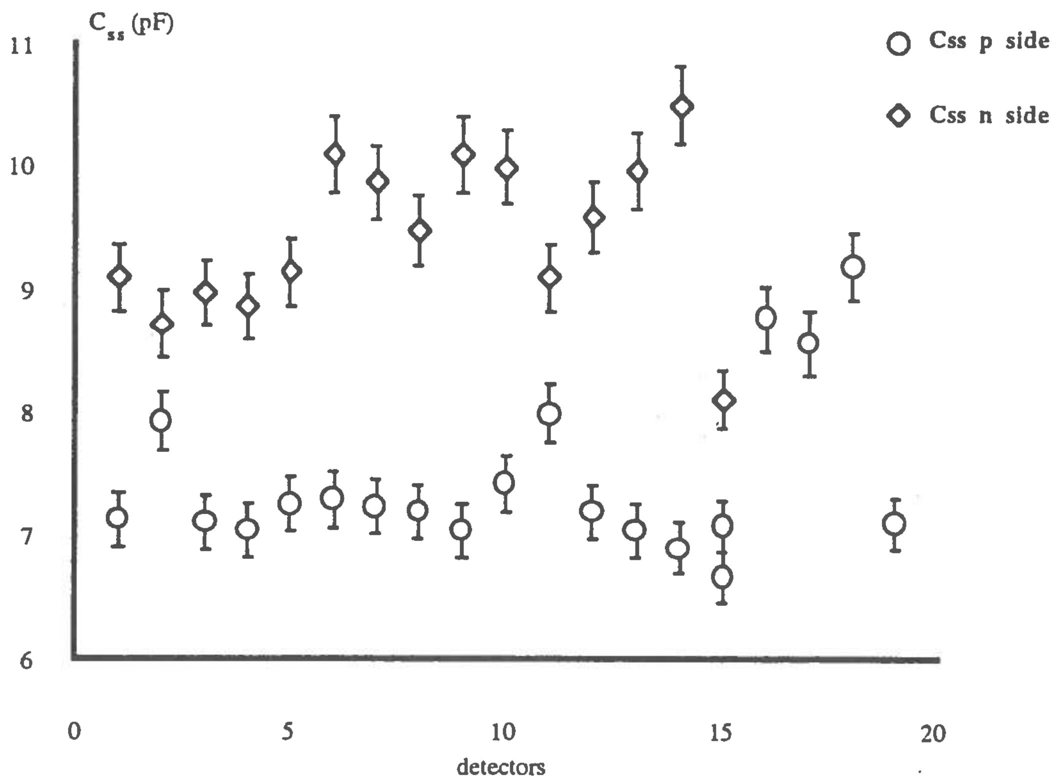


Fig.21 Values of C_{ss} for the p^+ and n^+ side sampled on different strips and different detectors.

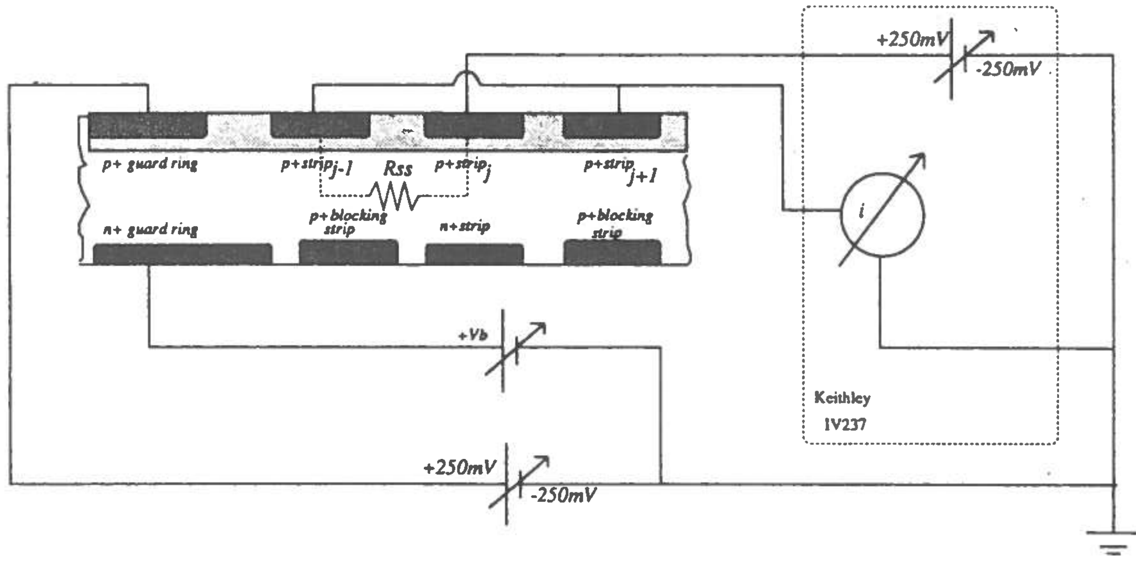


Fig.22 The set up for the measurement of the interstrip resistance. A similar set up is used for the n^+ side.

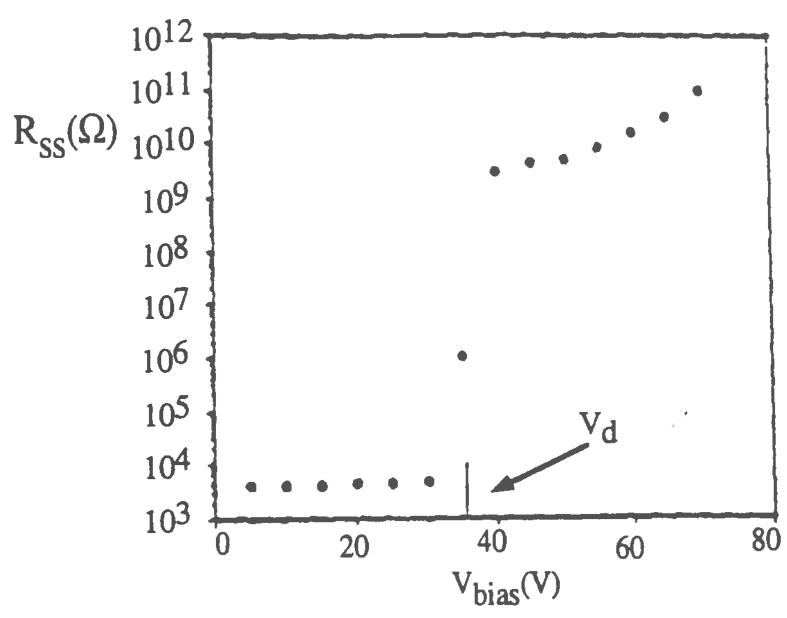


Fig.23 The curve for the n^+ interstrip resistance obtained from several IV curves at different V_{bias}.

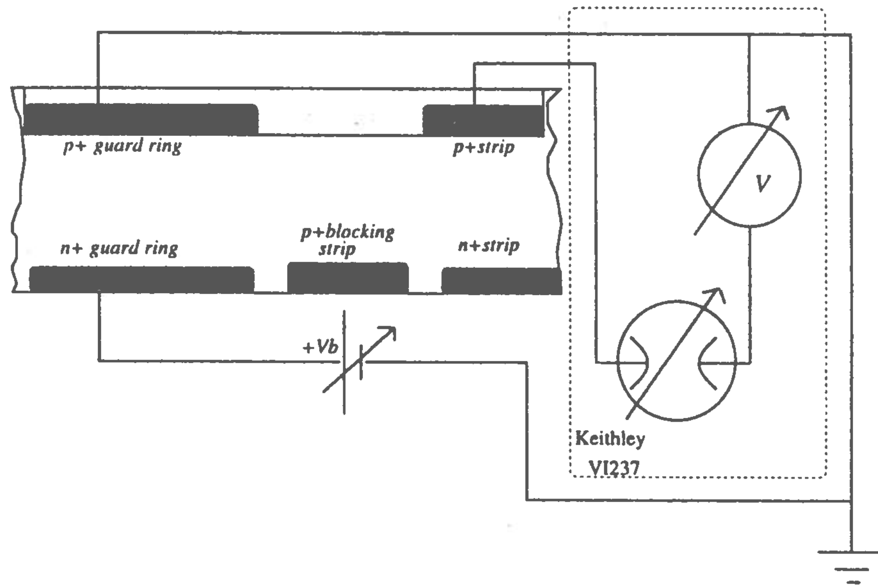


Fig.24 The set up for the measurement of the p^+ strip-guard ring, to measure the voltage drop. A similar set up is used to measure the voltage drop in the n^+ side.

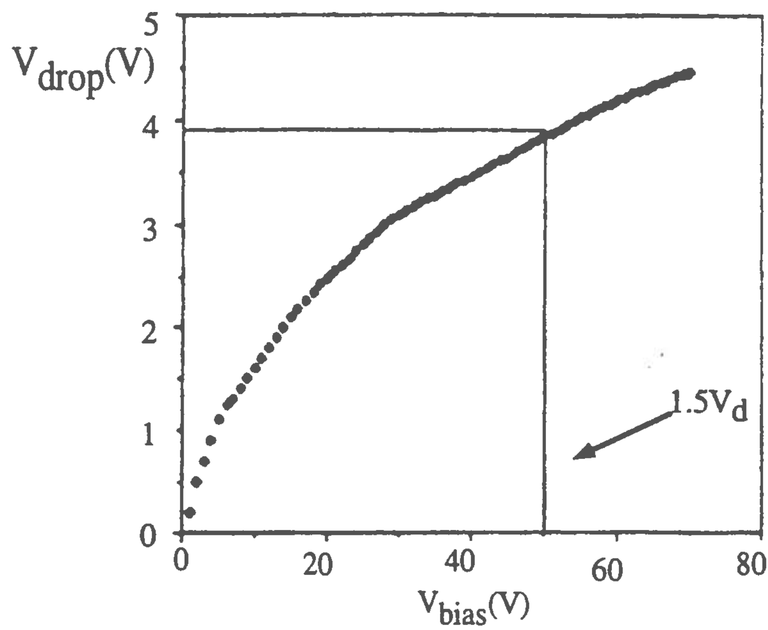


Fig.25 The p^+-strip-guard ring VI curve, to measure the voltage drop.

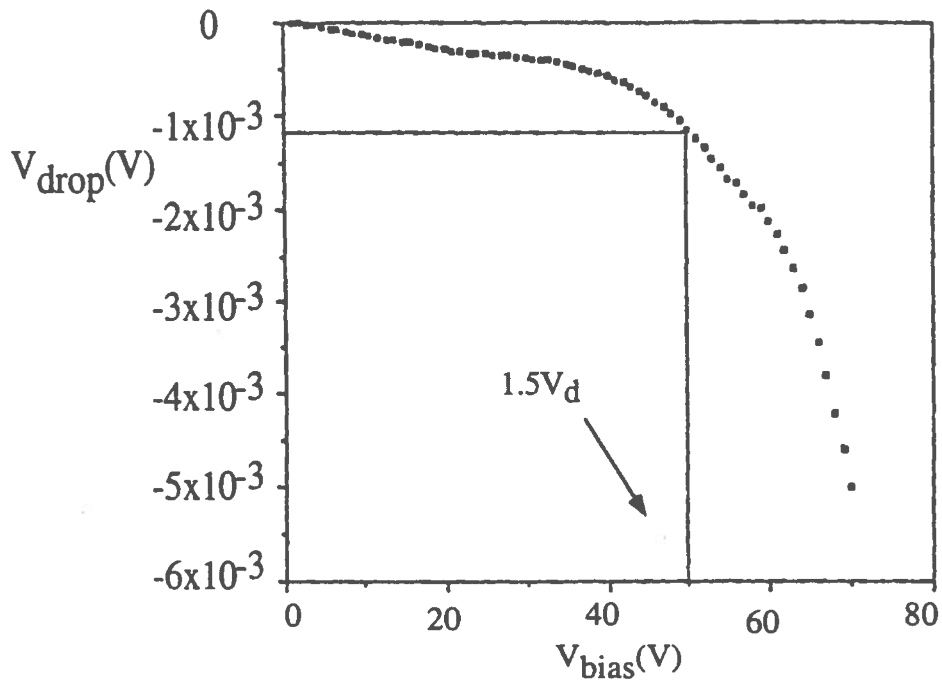


Fig.26 The n^{+}-strip-guard ring *VI* curve, to measure the voltage drop.

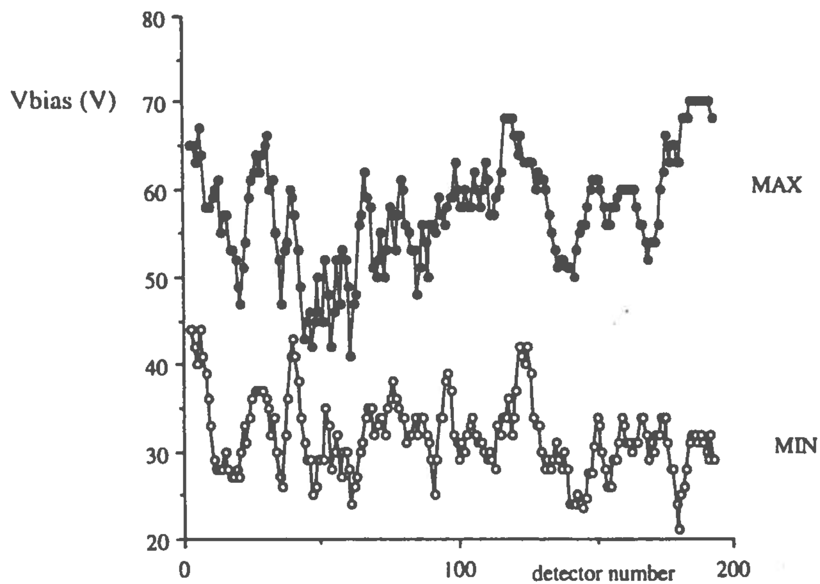


Fig.27 Illustration of the interval of bias voltage for safe operation for all the tested wafers. Full dots correspond to the maximum voltage below current instability, empty dots correspond to the minimum voltages for overdepletion.

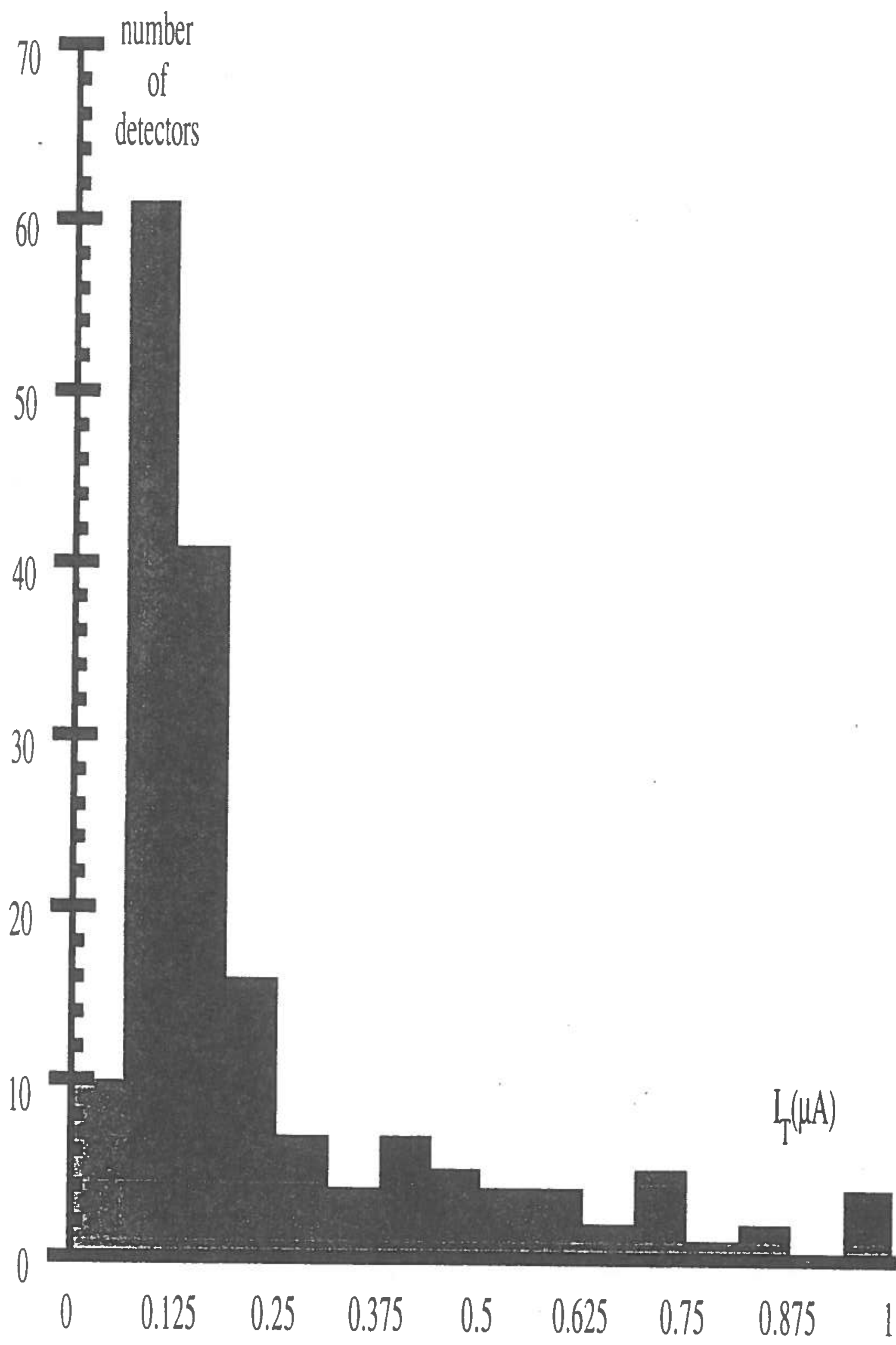


Fig.28 Distribution of the total leakage current at V_o for all the detectors with $I_T \leq 1\mu A$.

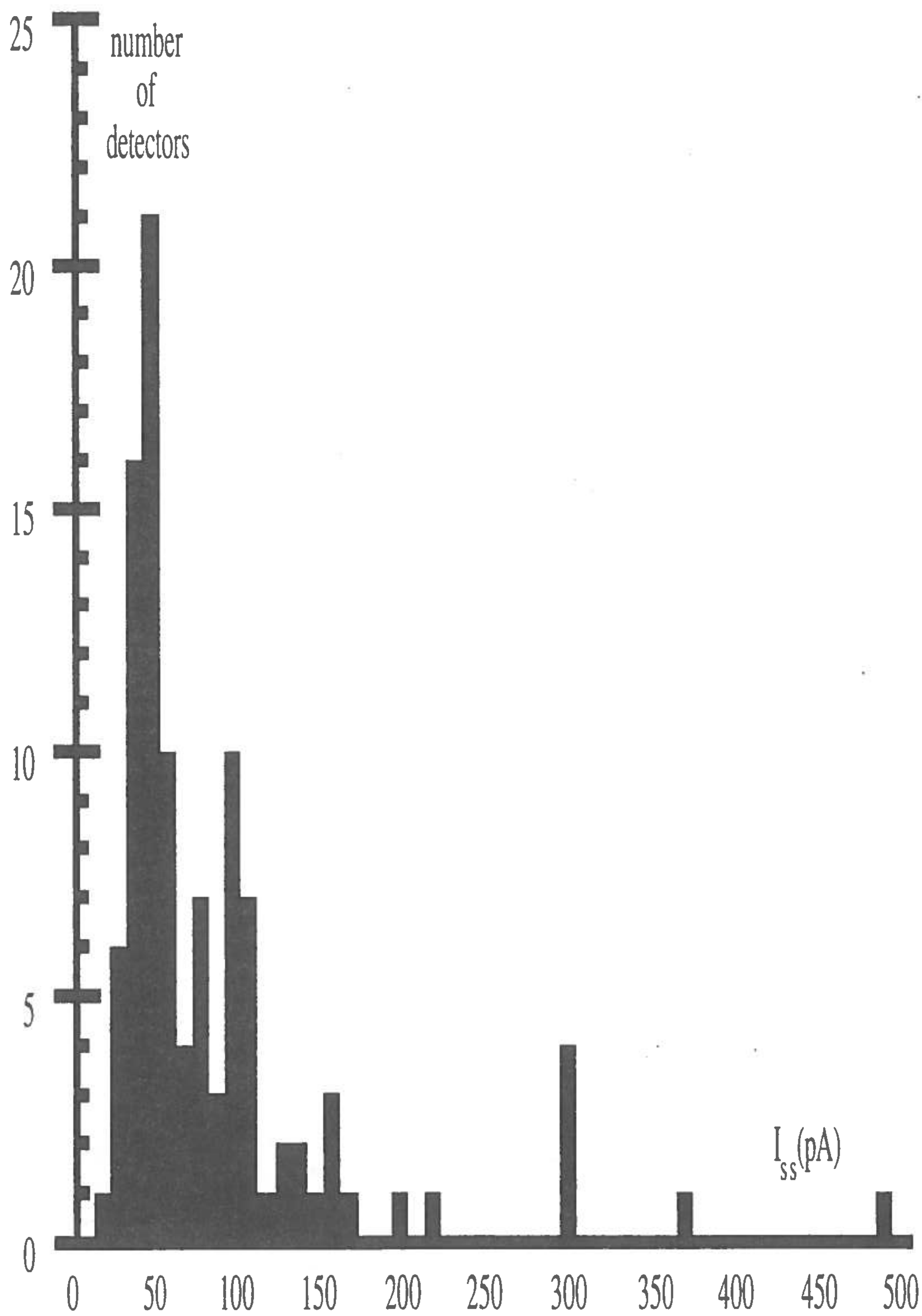


Fig.29 Distribution of the mean I_{ss} on the p^+ side sampled on all batches for detectors with $I_T<2\mu A$.

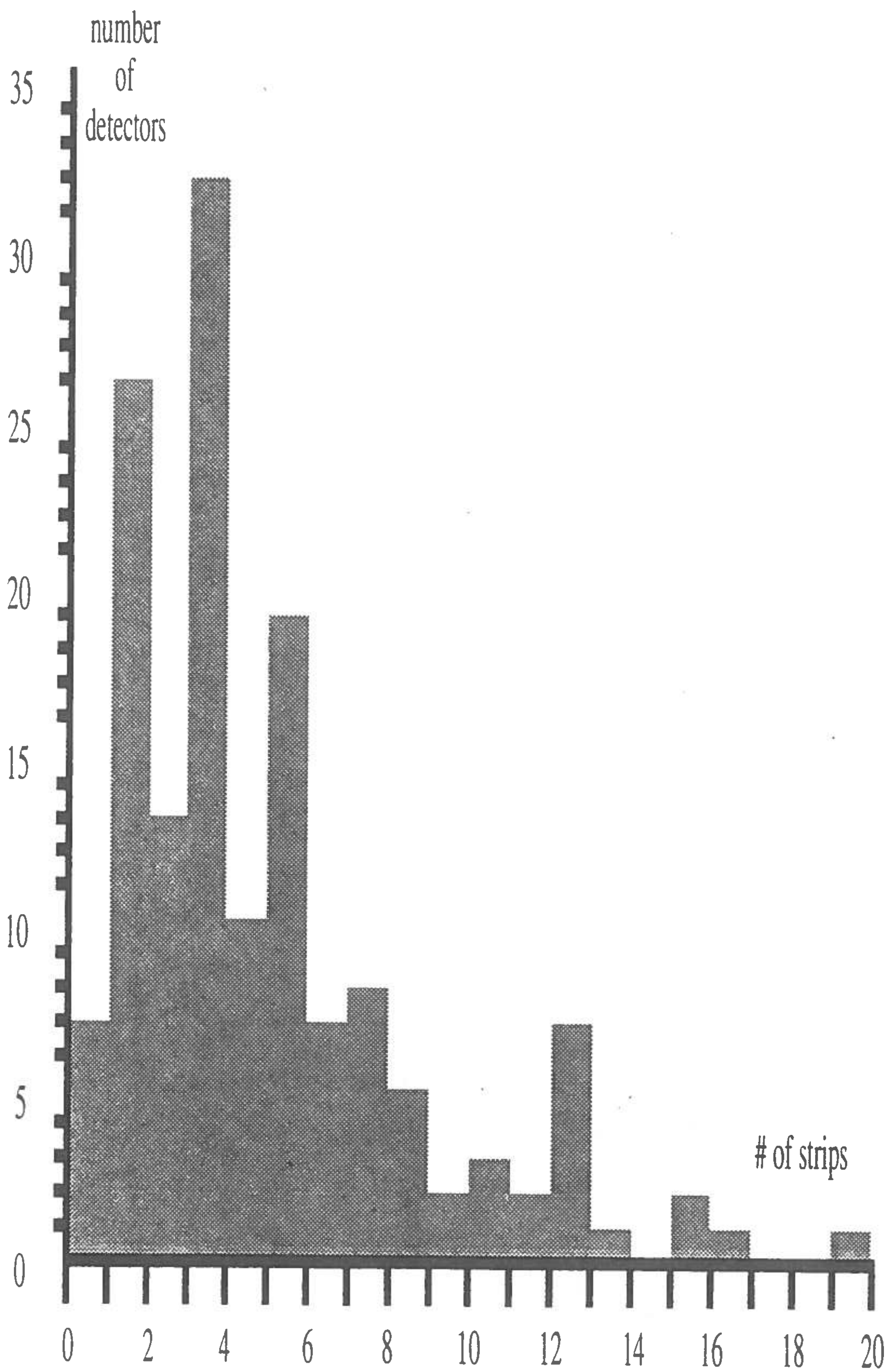


Fig.30 Distribution of the number of strips with $I_{ss} > 50nA$ on the p^+ side per each detector.

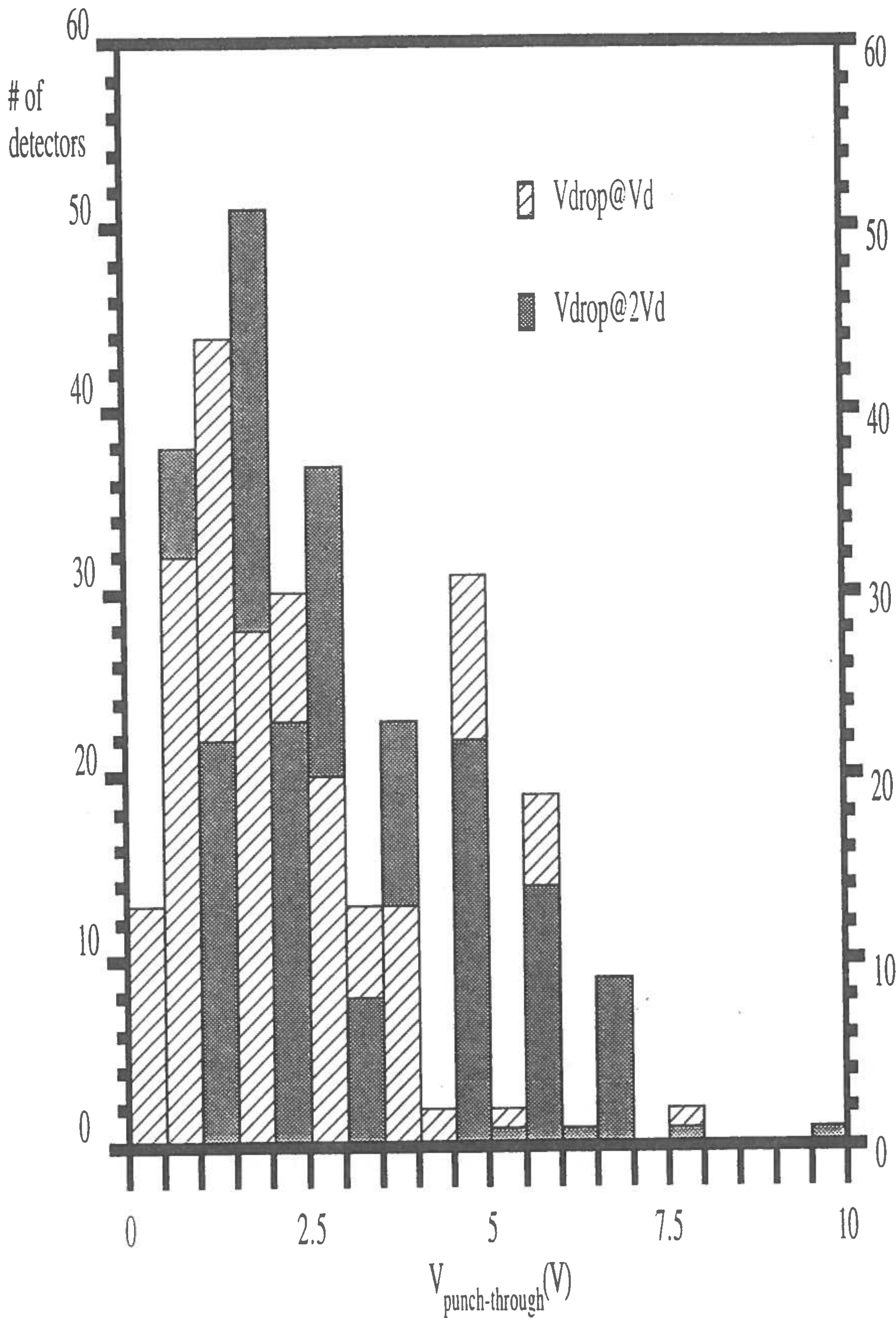


Fig.31 The distribution of the punch through voltages per detector in the p^+ side, measured at V_d and at $2\times V_d$.

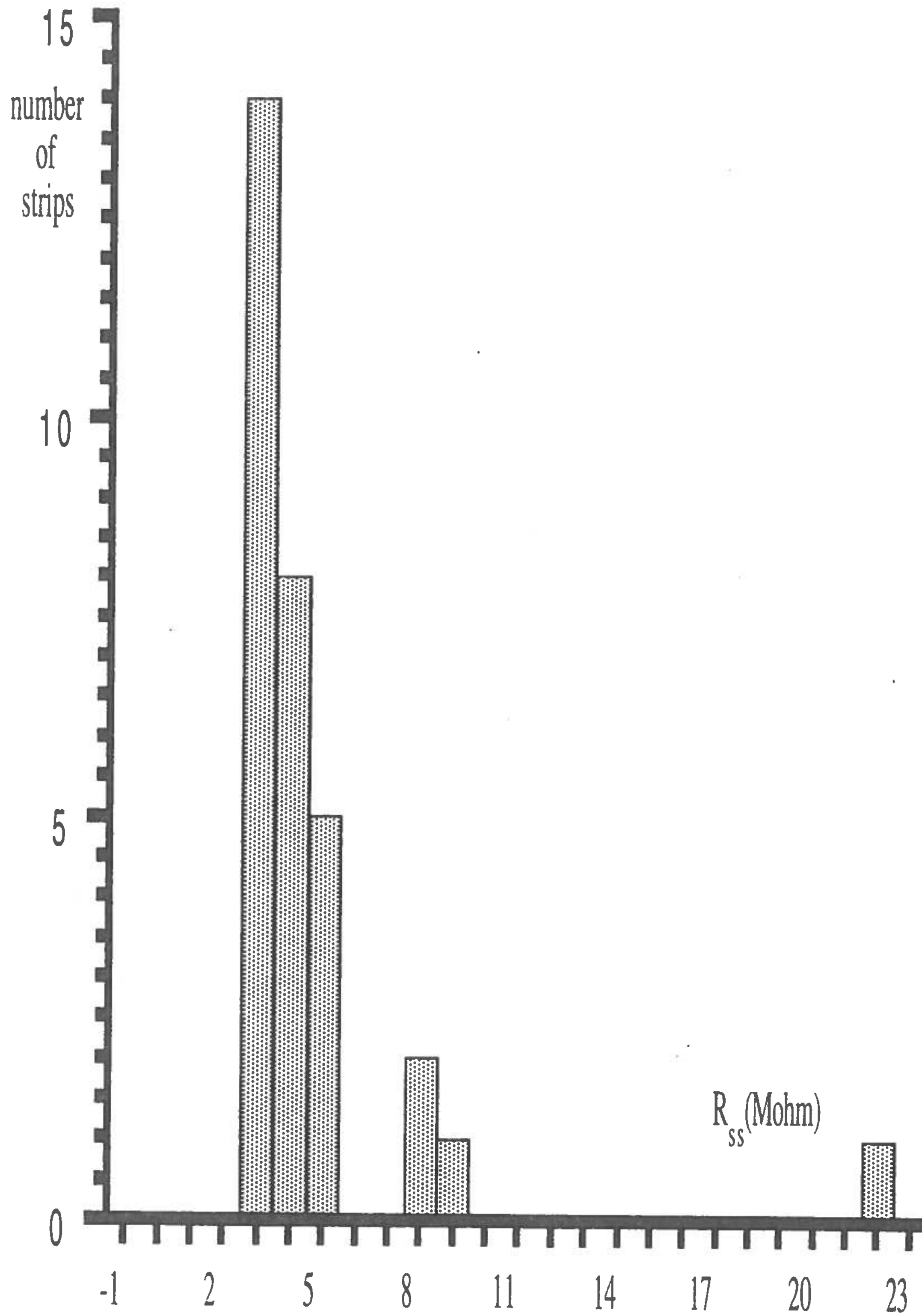


Fig.32 The distribution of the interstrip resistance per strip pair and per detector, sampled over the detector and over the batch, for several batches, in the n^+ side.

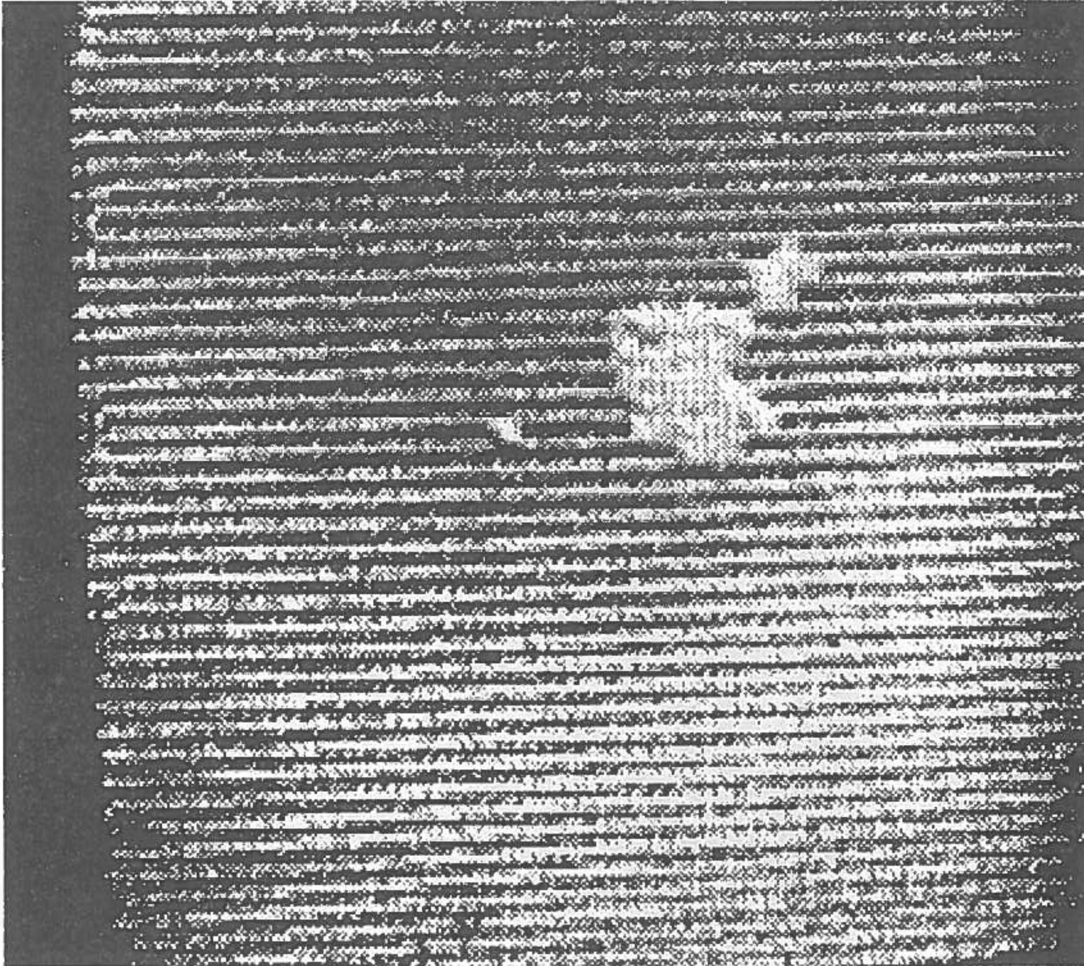


Fig.33 TV camera picture of the microscope image on pairs of strips of the p^+ side, showing high current. The spot visible, covering the region in between the strip, is aluminum deposit.

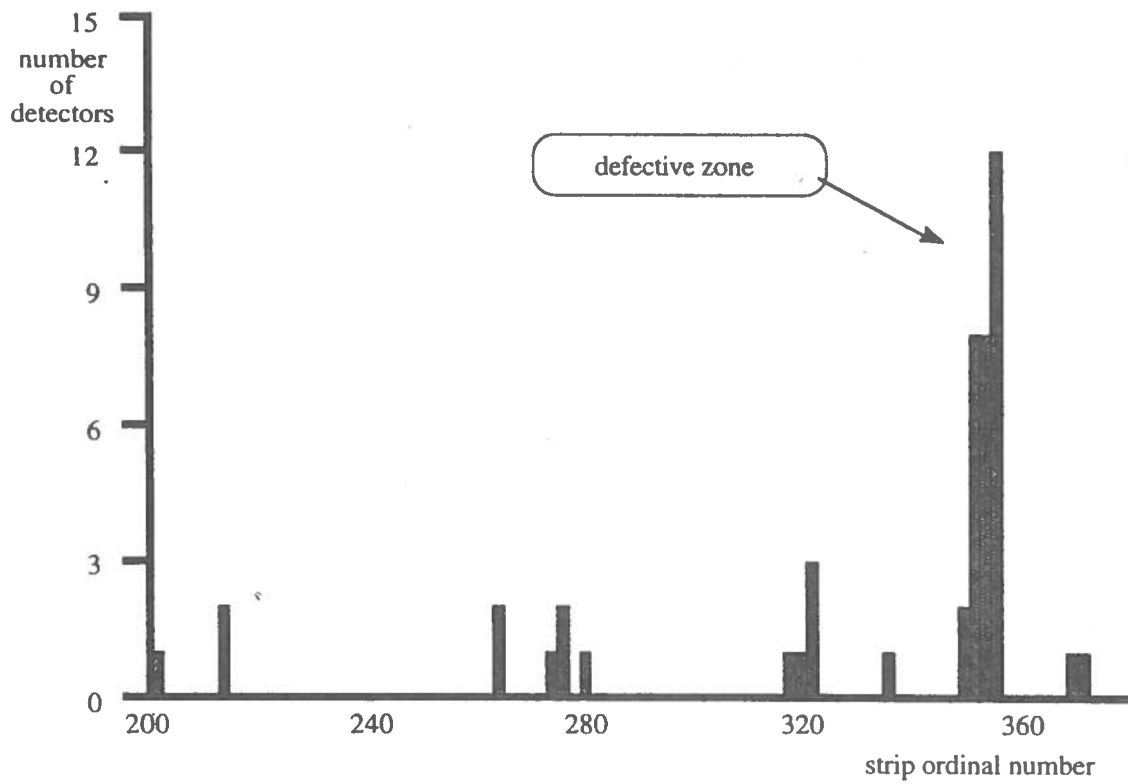


Fig.34 Plot of the number of times a detector has a strip with high I_{ss} in the p^+ side, versus the strip ordinal number for a defective batch.

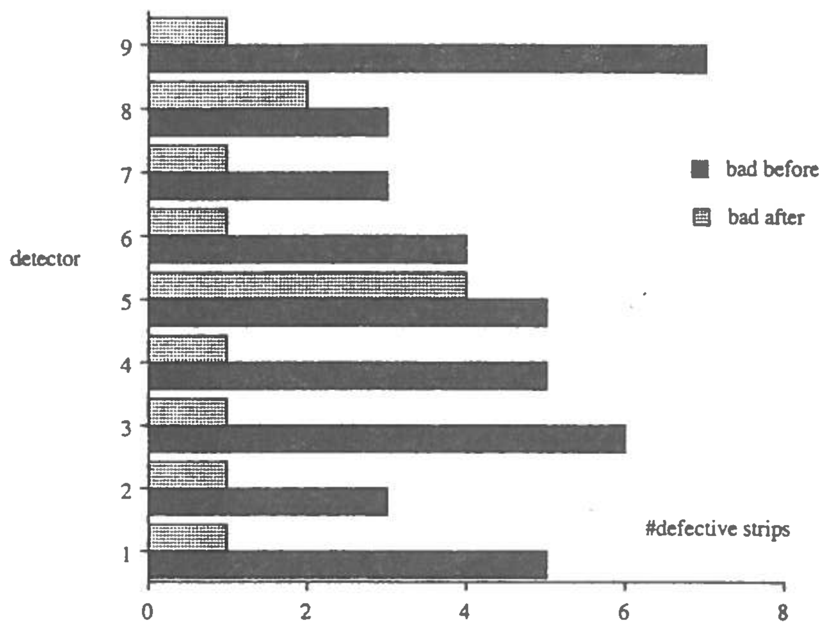


Fig.35 Number of strips of several detectors with large I_{ss} before and after intervention, for a trial batch.

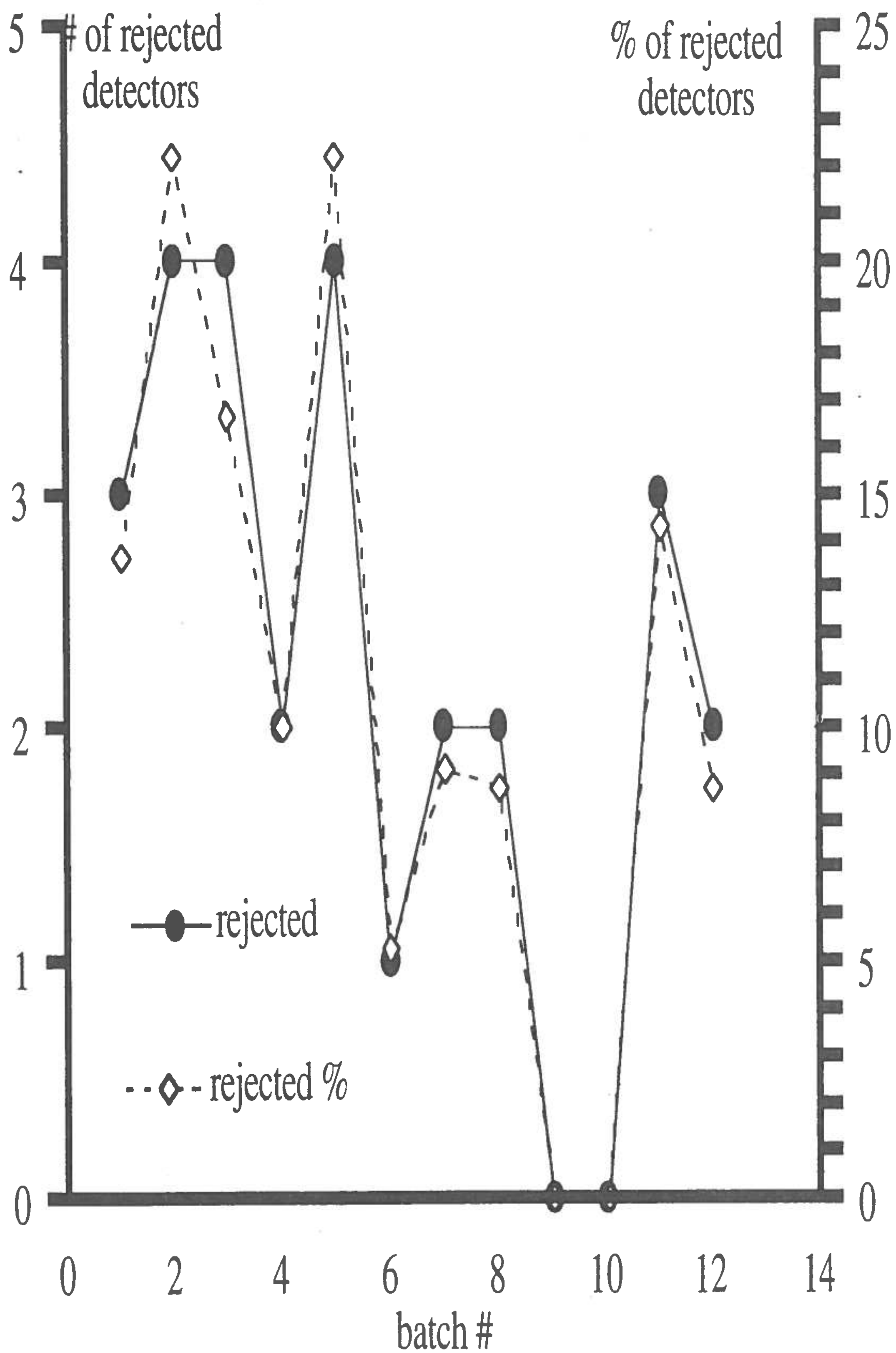


Fig.36 Number of rejected detectors (solid line) on the basis of the I_T leakage current criteria versus the batch number; dashed line is the percentage per all the detector of each batch.

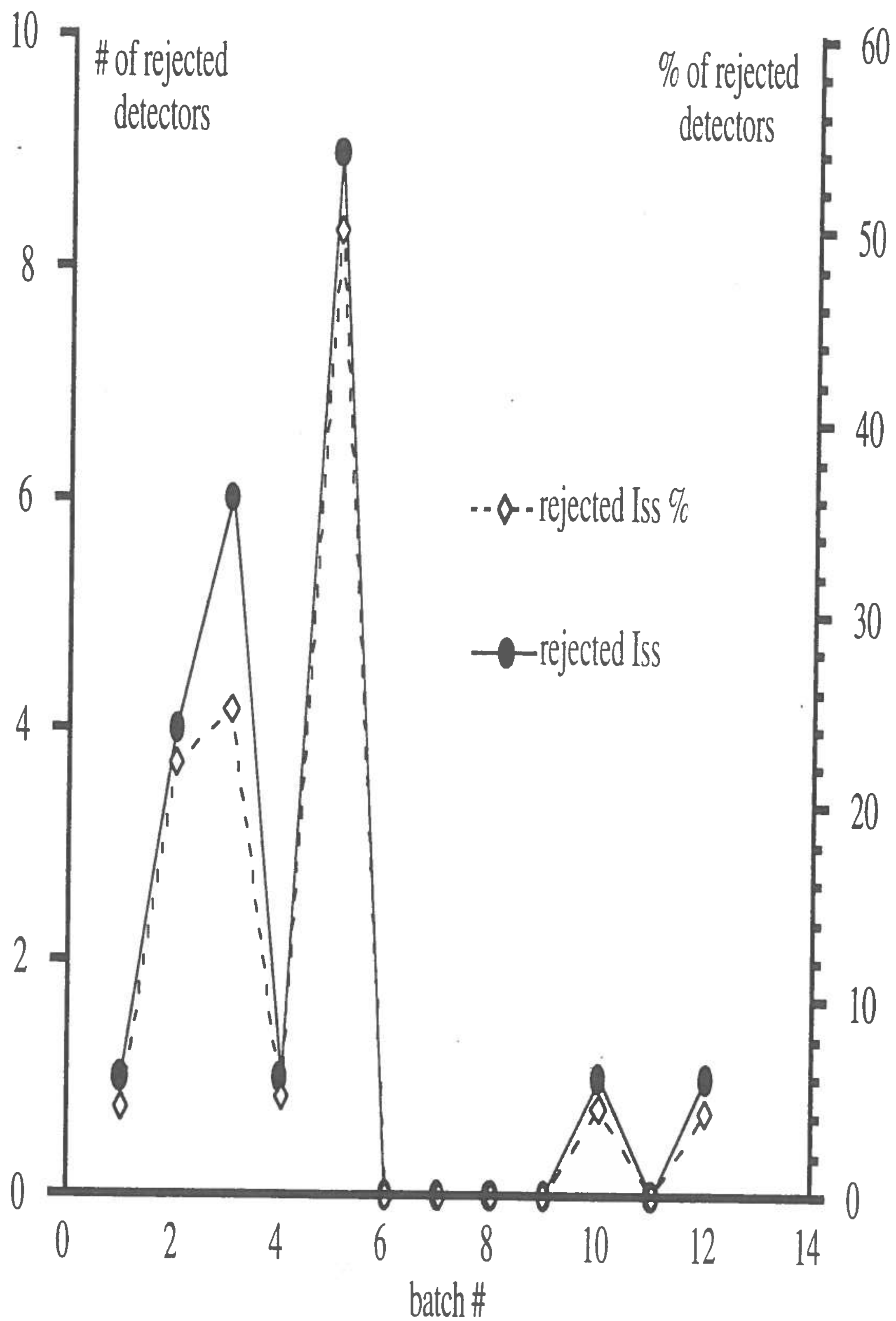


Fig.37 Number of rejected detectors (solid line) on the basis of the I_{ss} criteria versus the batch number; dashed line is the percentage per all the detector of each batch.

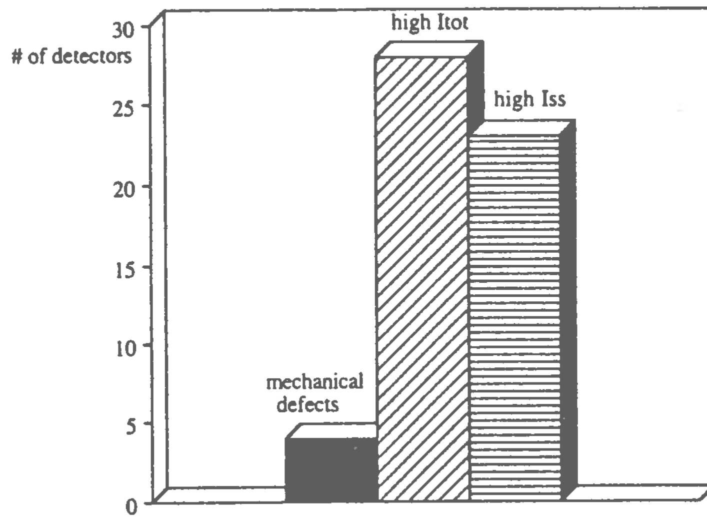


Fig.38 The total rejection rates disentangled by the three selection criteria.

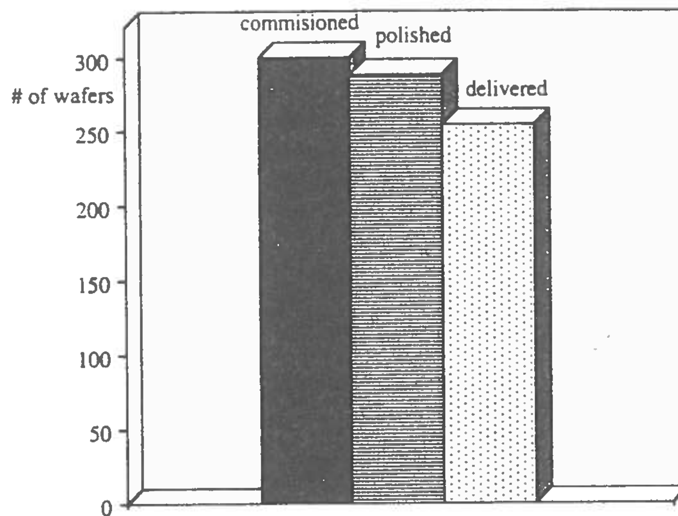


Fig.39 The number of wafers and detectors out of each fabrication step.

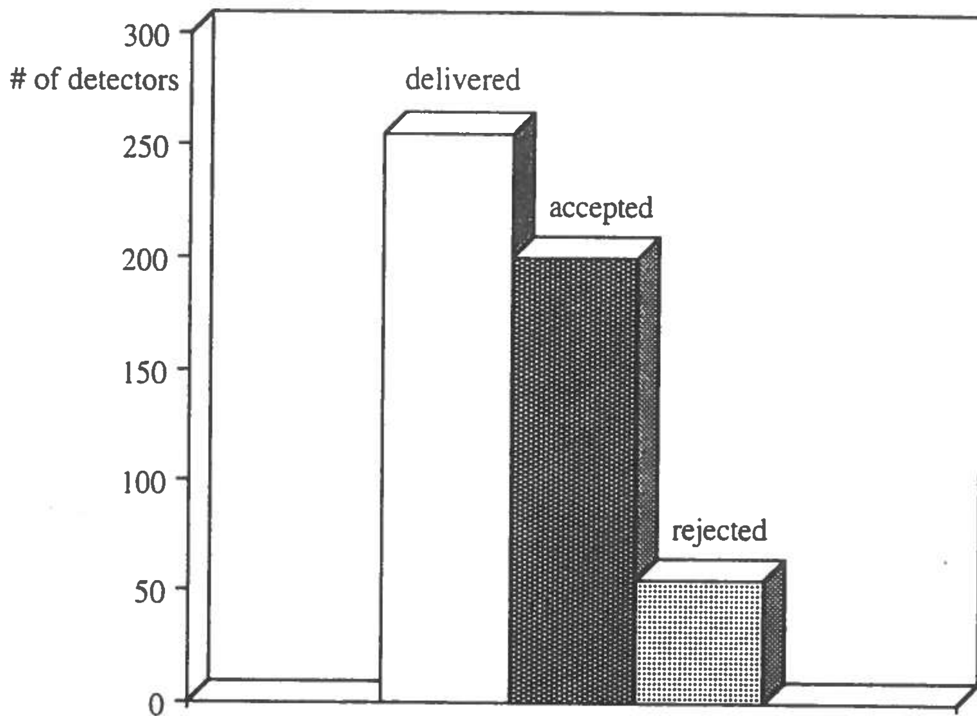


Fig.40 The total number of accepted and rejected detectors. The sum of the two bins, sums up to the first one, the number of fabricated detectors.