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TESTS OF A LARGE SCALE PRODUCTION OF DOUBLE SIDE SENSORS FOR THE L3 SILICON MICROVERTEX DETECTOR

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Abstract

Tests on a large series of factory produced double side silicon microstrip wafers are reported. Details of the set up, together with a description of a fast and reliable control procedure are given. More than 150 detectors were tested in less than 1 year time with an acceptance level of ≈75%.

I. INTRODUCTION

Tracking detectors based on silicon microstrip wafers are being used in many high energy physics experiments. In spite of their complexity and relatively high cost their superior performances indicate them also as excellent candidate for next generation hadron collider detectors[1]. There the dimensions will be such as to need a very large number of detectors, reliably constructed and tested at reasonable costs. in terms of manpower time and money. It is therefore relevant to acquire experience on the operation of a full chain system from the factory processing up to the final mounting.

Here we report on the production of a large series of double side microstrip wafers for the L3 experiment microvertex detector[2],[3] at the CERN LEP accelerator. We

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describe the measuring set up with computer control, we discuss and present results on the relevant parameters for a quality decision; we discuss the reliability and the time optimization of the procedures and finally we show results for more than 150 detectors.

II. THE DETECTORS

The detectors were realized on high resistivity (≈10kΩcm) n-doped silicon wafers[4], polished on the two faces[5], etching aluminum strips off the p^+ junctions on the SiO_2 substrates on one side and depositing the strips aluminization on the n^+ (or "ohmic") side with blocking p^+ strips[6]. To gain stability for the measurements, two guard rings were realized on the junction side, the inner being powered,working as a dc bus line via the punch-through current effect, to acquire the same potential on all the strips and compensate for the drops on the electronics readout lines.

The junctions side strip pitch is 25μm with aluminization as bonding pads only every 50μm, as the read out pitch. The n^+ strip pitch is 50μm all aluminized with bonding pads.

The dimension of the detector obtained in a 10cm diameter circular wafer of ≈280μm thickness is ≈4x7cm^2. The strip width is ≈10μm and the bonding pad is a rectangle ≈200μmx50μm. The strip length is 7,04cm in the junctions side and 3,84cm in the opposite side.

In the same wafer several test structures are fabricated to monitor the different steps of the processes, by determining the relevant parmeters for the quality control. In particular a circular diode implantation on the junction side, of ≈2cm diameters with two concentric guard rings, allowed to determine the depletion voltage V_d from capacitance measurements as described below.

We present here the results for 168 detectors for 8 batches of about 20 each, processed in ≈300 days time.

III. THE MEASUREMENTS

The functioning of each detector has to be guaranteed for long time as it has to be mounted in a structure to be installed underground to run for many months, continuously. It has therefore to be ensured a long term stability in its electrical characteristics. In addition, since it has to be assembled with other detectors of the same type and connected to common electronics chain for powering and reading out, the electrical parameters should checked to be omogeneous.

The response of a double side silicon microstrip detector working as a position measuring device, in "capacitive division" mode[7], depend on:

1- the *leakage current* of the single strip, which influences the electronics noise and, at the end, the position resolution of the detector;

2- the i*nterstrip capacitance and resistance* which influences the linearity of the response over the sensitive area, depending on the charge partition;

3- the *depletion voltage* and the *operating voltage* which must both be determined both to ensure the correct functioning of the detector in charge division and the quality of the wafer bulk;

4- the *voltage drop* as voltage difference between the guard ring and the strips on the junctions side, as it varies the omogeneity of the response from detector to detector and since they are assembled together, it must be set a priori like the operating voltage;

5- the *reverse current* of the whole detector measured at the junction side, as it is an index of stability and indication of noise sources different from the single strip leakage current.

The above mentioned quantities are directly connected to the macroscopic characteristics of the fabricated detector layers[8].

The detector must run at full depletion of free carriers in order to get the capacitive division method to properly work on both sides. This is done setting the bias voltage in the n^+ side at operation voltage $V_O=1.5V_d$, with V_d the depletion voltage, value determined by the capacitance measurement and directly proportional to the resistivity of the wafer bulk, i.e to the purity of the wafers. Under these conditions the reverse current of the detector can indicate the presence of surface charges, ascrible e.g to the improper cleanliness of the wafers.

The single strip leakage current measurement indicates the quality of the deposition processes of the implantation and of the aluminization in particular of the mask etching, in terms of their uniformiy in thickness and width. In addition possible isolated bulk defects can be localized. In presence of defective deposition of aluminum, even if simply non uniform, it is easily found that the single strip current is higher; if the aluminum defect causes some material falling outside the design dimensions (with tolerances of the order of 1μm), the leakage current shows values fairly higher than the mean.

The interstrip capacitance and/or resistance, depend, beside their geometric parameters, on the quality of the oxide layers surrounding the implantations. Inhomogeneity of the layers influence directly and locally the values of the interstrip resistance, while more extended defects can be appreciated on the capacitance value.

The voltage drop values are very sensitive to the guard ring-strip pads gap, eventually tunable as exposition time properly set at the design phase.

All the quantities mentioned above are therefore essential for the certification of this type of detectors.

IV. SET UP AND TESTING PROCEDURES

The quantities described before need extremely accurate devices, which for large number of detectors must also be highly reliable, fast and computer controllable. We have chosen Keithley[9] instruments for current, capacitance and voltage measurements, with GPIB interface to a personal computer, for which we have developed special software tools.

Delicate mechanical probing, to safely and reliably sense the aluminum strip pads and guard rings, was connected via low noise triaxial cables to the instruments. A schematic view of the se up is shown in figure 1.

The capacitance to determine the depletion voltage point was measured at a separate test diode of circular form with a concentric guard ring, implanted on the same junction side; the bias was applied on the bottom and the capacitance measured at 100kHz.

The measurement of the guard ring reverse current, had to be performed by sensing the inner guard ring of the junctions side, while biasing the guard ring of the n^+ side with positive voltage.

For the repetitive measurements of the single strip current, we have used a probe card[10] connected to a multiplexing device (Keithley 707) dedicated to the general control and switching of biasing and sensing. The procedure was, while biasing with positive voltage the n^+ side guard ring, to sense a strip and apply the same ground voltage to the inner guard ring and all surrounding strips. This testing scheme guaranteed the stability of the measurements except at the edges of the implantion mask, where the current tends to increase (figure 5, discussed later).

The capacitance of the single strip had to be measured with three probes to ensure adequate stability, by sensing the central strip and biasing the two adjacent to ground voltage.

The interstrip resistance had to be deduced by the slope of the IV curve obtained by varing the voltage between two adjacent strips from -250mVolt to +250mVolt, while biasing the detector over depletion.

The voltage drop between the strips of the junction side and the inner guard ring was measured by sensing one strip and the inner guard ring and biasing the detector at V_d and $2V_o$, after having verified that it was constant over many strips within 10%.

The typical values of the measured quantities are relatively small and subject to fluctuations, therefore the instruments sampling time and frequency had to be kept relatively high. This time must be added to the mechanical operations: for example for the junctions side the total time of the mechanical movements, the acquisition time and the recording time, was of the order of 90 min per detector. The average total time per detector, for the measurements of all the above characteristics, is

around 8 hours. However the resistance, the capacitance and the single strip current of the n^+ side, were sampled over one batch, reducing the characteristic time for the processing of one detector to 4 hours.

V. THE RESULTS

The bias voltage value at which the detector depletes, was determined via a least square fit of the capacitance vs bias voltage curve, by identifying the knee of the curve as the intersection to the two lines. In figure 2 the capacitance vs voltage curve shows how flat and long the plateau of depletion is, at relatively low voltage, indicating the high purity and factory conformity of the detector bulk, which allows easy pairing of the detectors in the structure and safe operation in a wide bias voltage range. This was not a parameter to certify the quality of the detector but it was mandatory to determine it per each wafer.

The first test for the certification was the measurement of the reverse guard ring current. A scan over a wide range of voltage was done (figure 3) to ascertain the stability of the detector and get the current values for the relevant corresponding voltages V_d, V_o=1,5V_d and 2V_d. Typical values at V_o are of the order of ≈150nA (i.e. 5nA/cm^2): these, as shown below, are fairly acceptables as they indicate the current is essentially build up only out of each single strip dark current contribution. If a detector had a current equal or higher than 2μA, was tagged bad. However, as it is shown in figure 4, the number of the detectors at this threshold are few as most of them cluster around 120nA, and the ones "bad" are mostly far above the acceptance cut of 2μA.

Usually the high current values indicate a high single strip current but to detect noisy strips with currents even orders of magnitude higher than the expected junction dark current, it was necessary to scan over each strip for the junction side and in order to save time to sample per batch the n^+ side strips. As it can be seen in the example of figure 5, the dark current of the single junction, fairly stable over >700 strips beside the mentioned smooth geometrical measuring effect at the edges of the detector, was around 50pA, i.e., being not larger than the typical electronics noise of few hundreds of electrons, fairly acceptable. A strip with current higher than 50nA was identified as "noisy". Usually the noisy strips are adjacent because of the defects of the implantations or of the lithography. If a detector had more than 2 noisy strips, it was tagged "bad". The same occurs therefore if there are more than two pairs of "bad" strips even if the defect could be localized and seen in one strip only as the read-out pitch of the detector is 50μm.

The value of the interstrip capacitance changes dramatically with bias voltage. In particular it has no meaning if the detector is not depleted (figure 6), as there are free charges in between two adjacent strips. Then, to check the quality of the detectors,

the values of the capacitance had to be measured at bias voltages greater or equal than V_d, for both, the junction and the n^+ side. The values shown are as expected purely dependant on the geometry of the strip[11] with a value of ≈1,3pF/cm omogeneous over many detectors.

Since the most delicate part of the processing was the n^+ side, the quality check was performed systematically only there, sampling a wafer per batch. A fixed cut was not applied, as it was sufficient to measure the interstrip resistance: as reported below the value for the detector in figure 7 indicates that the capacitive division read-out method can be used.

Curves with several interstrip resistance values at various voltages were taken. The global curve at V_O, like the one in figure 7, was obtained: this quantity is clearly not fixed until depletion is reached. Fairly high values are expected for the p+ as the crystal was of type n: with our apparatus we could establish a limit of $R_{SS}>2G\Omega$. The n^+ side, was systematically sampled. The criteria for tagging the detector "bad" was an interstrip resistance in the ohmic side $R_{SS}<2M\Omega$.

In summary a detector was tagged as "bad" if:

1) the reverse current at the guard-ring in the junction side $I_{gr}\geq 2\mu A$, or if

2) the number of noisy strips of the junction side (eventually also of the n^+ side) was ≥3, or if

3) the interstrip resistance in the n^+ side was $R_{SS}<2M\Omega$.

In figure 8 the values for 168 processed detectors are represented with the number of detectors rejected under the above criteria; it is remarkable to notice that no detectors were rejected under criterium 3). The overall acceptance rate was 75%, extremely high for double side wafers with more than 3000 implanted strips. This indicates the excellent quality of the factory processes and that the double side technique is reliable for a large number of detectors.

VI. SUMMARY

A large series of double side microstrip silicon detector has been tested for quality certification. The tests performed were reliable and relatively fast. In less than one year time 168 detectors were produced and tested. The certification was done on the basis of the reverse leakage current, the single strips current and the interstrip resistance, for the junction and the n^+ strips. The depletion voltage, the voltage drop from guard ring to strips and the interstrip and bulk capacitances were also sampled. More than 75% of the total were detectors with fairly good characteristics, well below the acceptance criteria: typical values were a reverse leakage current and a single strip current ≈5nA/cm^2 and interstrip resistance in the n^+ side >> 2MΩ.

With these results, experience has been gained to show that the double side silicon technicque can be mastered and controlled in a fast and reliably manner, indicating it

as an excellent candidate for the large area detectors at future high energy physics experiments.

VII. ACKNOWLEDGEMENT

We gratefully acknowledge the continuous advises of Professor L.Bosisio.

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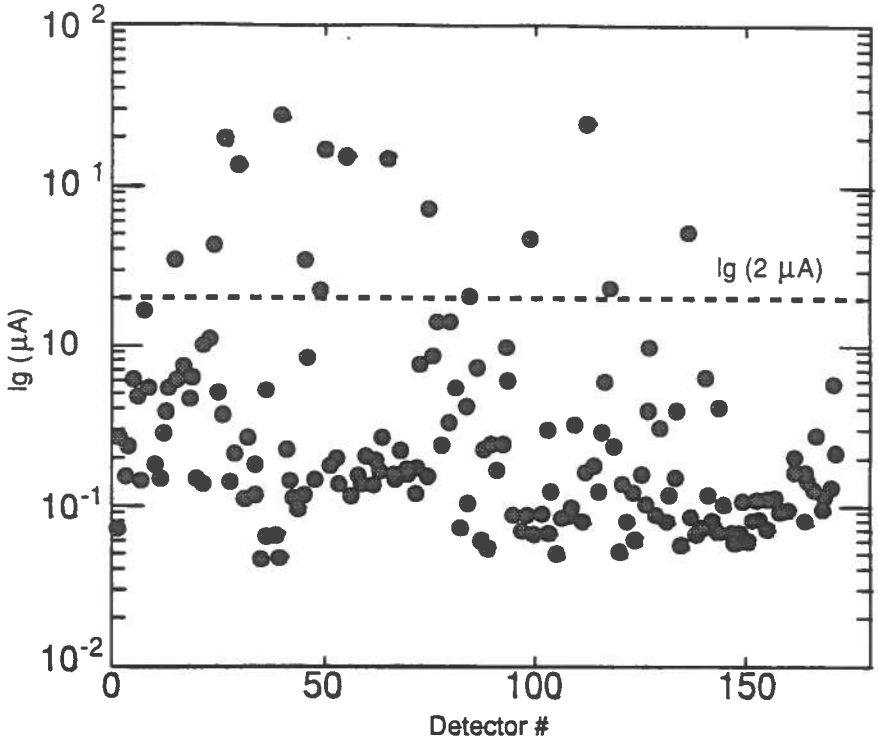

Figure 4: The distribution of the reverse currents measured for all detectors

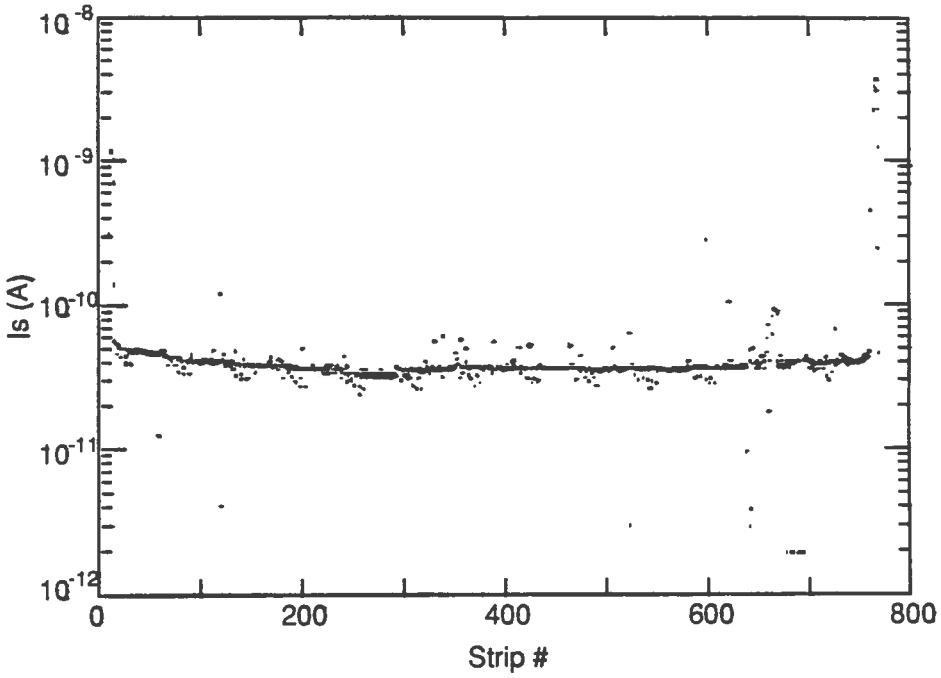

Figure 5: The measurements of the single strip current at the junction side for one detector. The measurement was done in a single shot at V_0 for each detector.

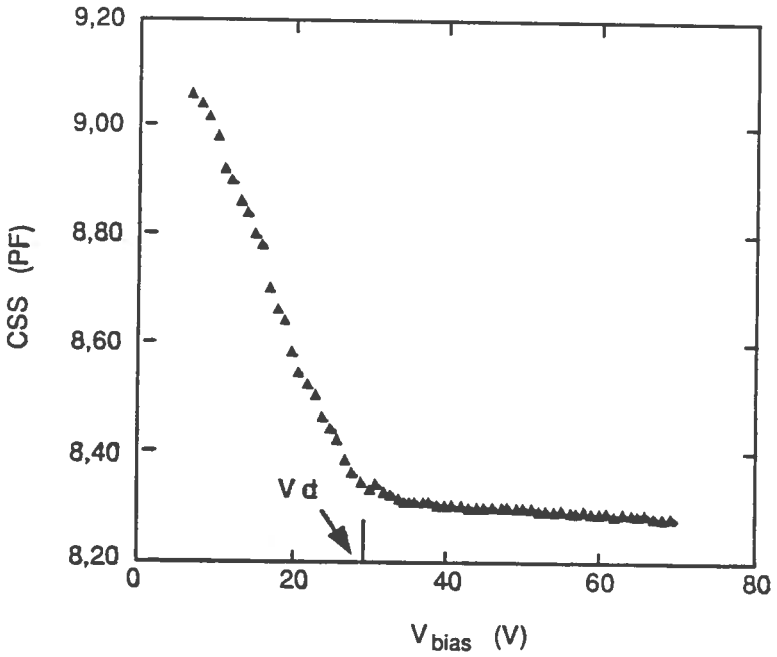

Figure 6: A typical curve of the interstrip capacitance at the junction side vs V_{bias} .

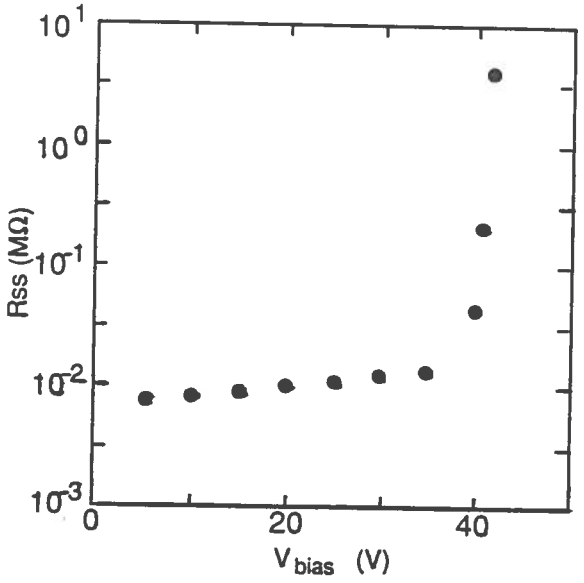

Figure 7: The n^+ side interstrip resistance

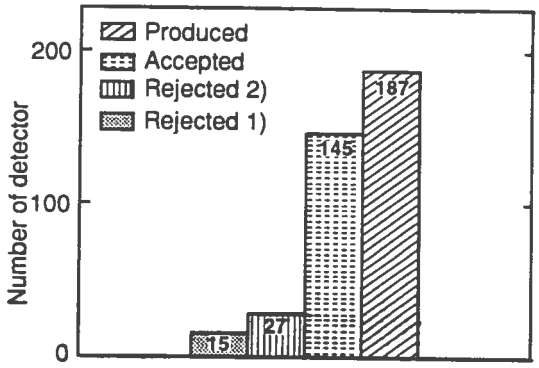

Figure 8: Plot of the different classes of detectors: the detectors rejected because of the three different criteria (see text) are indicated: together with the accepted ones, they sum up to the total detectors processed.

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