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M. Caccia, P. Guazzoni, W. Kucewicz, C. Meroni, G.F. Taiocchi, G. Vegni, L. Zetta

**A FAST ANALOG-TO-DIGITAL READOUT  
FOR MICROSTRIP DETECTORS**

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A fast analog-to-digital readout for microstrip detectors

Massimo Caccia(1), Paolo Guazzoni(1), Wojtek Kucewicz(1,2),  
Chiara Meroni(1), Gianfranco Taiocchi(3), Guido Vegni(1),  
Luisa Zetta(1)

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(1) Dipartimento di Fisica dell'Universita' and Istituto Nazionale di Fisica Nucleare - via Celoria 16 - 20133 Milano - Italy

(2) On leave of absence from University of Mining and Metallurgy Ul. Czarnowiejska 78 - Krakow - Poland

(3) Ditta Takes - Ponteranica Bergamo - Italy

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ABSTRACT

An analog-to-digital fast readout, using a 8-bit flash ADC, for DC-coupled microstrip detectors, has been developed with automatic pedestal and offset subtraction. The system (readout + detector) was preliminary tested with special pulsers, beta-sources and, at the end, in a minimum ionizing particle beam. The performance and the experimental results obtained are similar to conventional systems employing larger dynamic ADCs.

## 1) INTRODUCTION

Silicon microstrip detectors are now worldwide employed in high energy physics experiments, where very good spatial resolution is required.

In particular, in case of collider experiments (1-5), vertex detectors using a huge number of readout channels (about  $10^5$ ) has been designed. Due to the severe limits imposed by space, power dissipation and material considerations, VLSI readout chips, able to match the high density of strips, have been developed.

Using conventional detectors (DC-coupled) with VLSI-multiplexers (6-8) -as well known - the leakage currents of individual strips can give troubles to data taking. In fact the leakage currents of individual strips often vary by a factor of up to 1000 across one detector. This does not in general affect the spatial resolution as long as the leakage currents are  $\leq 200\text{nA}/\text{strip}$ .

With chip readout this phenomenon can introduce large baseline differences (DARK PEDESTAL) between different channels of the same chip and usually requires a Fast ADC of large dynamics (10-12 bits), otherwise unnecessary. Moreover the use of chips can often introduce sudden variations of the zero level (OFFSET) of the signal for all the strips. This variation is the same for all the channels of the same chip.

An answer to overcome these problems can be now given by the AC-coupled detectors (9), but the presence of the capacitive coupling of the diode strips to the metallization gives a limit to the minimum reachable pitch -25  $\mu\text{m}$  up to now (9)- with respect to the 10  $\mu\text{m}$  pitch (10) of DC-coupled ones.

In the case that this minimum pitch is required ( for example see ref. 11), the use of DC-coupled detectors is necessary.

We have therefore designed built and tested a fast analog-to-digital readout, MIDAS (MICROSTRIP DETECTOR ANALOG-TO-DIGITAL SYSTEM), firstly announced in ref. 12, with the aim of exploiting some peculiarities of the analog electronics to make a first manipulation of the data -e.g. pedestal and offset subtraction- during the acquisition. So, the signals being decreased of the DC-pedestal, an 8-bit accuracy is enough, directly allowing the use of commercial Flash ADC. So it is possible to read a strip in only 400 ns, without using high speed components

(usually needing high power consumption) and reducing the size of the circuit, without heat dispersion problems. In the following the physical constraints for the design (Section 2), the general description of MIDAS (Section 3), the performance and experimental results (Section 4), will be given.

## 2) PHYSICAL CONSTRAINTS

While MIDAS could be easily adapted to different configurations, the major part of the constraints we had to face are typical of DELPHI readout structure. In fact originally it has been designed as an alternative solution to the DELPHI Vertex Detector readout. The DELPHI Microvertex is described elsewhere (13,14). The original main characteristics of its readout to be taken into account are as follows.

The pitch is 50  $\mu\text{m}$  and the total number of channels is  $\sim 50\text{K}$ . The readout electronics, realized with a 5 $\mu\text{m}$  VLSI technology is a 128 channel chip.

Each channel consists of a charge sensitive amplifier with correlated double sampling and holder for noise reduction (Microplex) (6). All the 128 channels are time multiplexed on a single output via a shift register and a differential amplifier. Many chips can be chained and again multiplexed and are controlled by an unique driver.

The sequence of signals during the readout is shown in fig.1. Clock 1 and Clock 2 drive the read bit along the shift register, the maximum frequency being limited by the settling time at the output of the differential amplifier that is, in our case, between 200 and 300 ns per channel, the maximum speed is around 2.5 Mhz.

The microvertex readout had to fit into the more complex DELPHI trigger and readout scheme (14). DELPHI has a 4-level trigger system, the first 2 levels are synchronous with the beam cross over (BCO) (every 22 $\mu\text{s}$ ).

The trigger decisions occur in 3 and 40  $\mu\text{s}$  after the BCO for the first and second level respectively.

The subsequent levels are asynchronous with much larger processing time (>30ms).

After the 2nd trigger the preliminary readout phase starts, to have all the front-end buffers ready for the next event. The time for transferring the data to some intermediate buffer is 500  $\mu$ s and all the operations needed for data clustering and compression have to be completed in 3.5 ms.

### 3) GENERAL DESCRIPTION

To satisfy the constraints previously stated, MIDAS was designed, built and tested.

The main items MIDAS try to achieve are:

- a) high reading and conversion speed;
- b) automatic subtraction of the pedestal, continuously following its variation during the time. The range of this stabilizer is 10-20 times greater than the signal dynamics;
- c) automatic correction of sudden variations of the offset coming from Microplex.

Moreover a single module of MIDAS is designed to process, with differential inputs, up to 1024 strips, divided into 8 Microplexes.

The MIDAS prototype was realized using wire-wrap technique, with no arising problems also if the main clock frequency is 20 MHz, and commercial HCMOS components are used.

A first simple description of MIDAS can be given following the front panel shown in fig. 2.

The scanning delay ten turn potentiometer is used to synchronize the strip scanning with the conversion frequency. Moreover the fast/slow scanning toggle switch allows to change the scanning frequency, introducing a 1  $\mu$ s pause between two cycles.

Two different toggle switches allow the pedestal and offset correction. Three Lemo connectors are used for scanning and differential input signals. Two BNC connectors allow the inputs of the 1<sup>st</sup> and 2<sup>nd</sup> level trigger signals. The test or operation mode is allowed by the proper switch. A 20-pin Amphenol female connector is used to present check point output signals.

Two 25-pin Canon connectors (not operating in the prototype) are foreseen for the digital and analog detector inputs. The first one can be foreseen for digital inputs coming from a special digital pulser, BIG (15), in order to check MIDAS,

starting after the ADC. The second one can operate, instead of the Lemo and BNC connectors, to have a more compact input of the analog and control signals, together with other control or trigger pulses, eventually needed.

The general MIDAS working mode can be easily understood following fig. 3. MIDAS, in fact, could be symbolically subdivided into five ideal sections (ANALOG INPUT, CONVERSION AND UPDATING, TIMING AND CONTROL, MEMORY AND DIGITAL OUTPUTS), each of which carries out a particular program of work, also if, topologically speaking, they can not be considered as a block.

### 3.1) The working sections

---Analog input: the aim of this section is to collect the analog signals coming from the Microplexes, in differential mode, and to perform the pedestal analog subtraction, using the values coming from the pedestal memory, properly converted from digital to analog. The external monitor output, which can be easily connected to an oscilloscope, is particularly useful, specially for an immediate evaluation of the pedestal correction. We have to remark that the zero value corresponds for MIDAS to the half value of the full range, allowing the correction of positive and negative sudden variations of the offset. The ADC input has a dynamical range of 0-5 V, easily adjustable changing the input resistor values.

---Conversion and updating: this section is entrusted with the task of completing the data analog-to-digital conversion (using a 8-bit flash ADC), the pedestal digital-to-analog conversion (using a 12-bit ADC), in order to allow the analog subtraction previously seen, and also to update the data memory after the proper corrections. The conversion is preceded by a wait. It interrupts all other operations at the point they are, storing the working address. In this way, at the end of the conversion, any operation is resumed at the same point.

---Timing and control: the main timing signal arises from a 20 MHz clock and a 8-step shift register with a cycle of 400 ns per operation. The first half part of this interval is used for the pedestal reading and the second one for writing the conversion results. The memory addresses used have the same

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content for the first ten less significant bits (LSB); the bits 11 and 12 are low. The 13<sup>th</sup> bit is equal to zero during the first 200 ns; equal to one for the remaining time (200 ns).

---Memory: in order to improve the reliability of all the system, the memories employed for MIDAS are not of FIFO type, but 8K-RAM memories with common address. 1K of memory is used for pedestal zero level, while 4K are employed as event buffer. The offset memories are 64-bit RAMs. Three address latches -one for each cycle- allow to respect the priority. So each operation can be stopped and restarted as soon as possible, without any loosing of memory. The memory for the converted signals, arising from Microplex, (data memory) is able to store (at the high rate required, about 400  $\mu$ s/1024 strips) the data corresponding to four different sequential triggers.

---Digital output: the output works in handshake with the external memory of the data acquisition system (MCA or SIROCCO III (16) in our case), either in list or increment mode, depending on the toggle switch in the front panel. In output we can have a 12-bit word representing either the data or the pedestal values, also in this case depending on the front panel toggle switch.

### 3.2) The working cycles

The data manipulation for each trigger is completed by MIDAS during three cycles (fig. 4), summarized in the following.

---First Cycle (required time 400 ns/strip): the pedestal memory is read. At the first time the values can be zero or the existing ones (coming from the previous trigger). The corresponding values are then converted into analog signals to allow their analog subtraction from the input signals (coming directly from Microplex). The results (INPUT SIGNAL minus PEDESTAL VALUE) are amplified (G=6.8) and converted with an 8-bit accuracy. This accuracy is enough, as previously related, because now the analog signal to be converted has been decreased of the pedestal value. The digital data are stored into the DATA MEMORY.

Successively the offset values - eventually introduced by the Microplex read-out chips - are computed and stored (OFFSET MEMORY).

---Second cycle (required time 800 ns/strip): during this cycle, the offset values, previously stored, are used for the data correction. In fact the data memory (where are stored the digital values of the difference between the input signals and the pedestal levels) is again read, and the offset value is subtracted up to a 7-bit accuracy. The corrected data are rewritten into the data memory. The cycle ends making the first upgrading of the Pedestal Memory.

---Third cycle (required time 800 ns/strip): The Pedestal Memory is again refreshed, the "good" data are reread and transferred. Also the pedestal values can be transferred, if required.

### 3.3) The working operations

In order to better understand the MIDAS structure we shall describe it, having in mind the three most important operations completed:

CONVERSION, REREADING and UPDATING, TRANSMISSION.

The severe timing of the whole system requires a hard synchronism between detectors, driver box and conversion unit. So the command for microstrip scanning is given by the driver box. The consequence is a certain delay between the scan signal input and the analog ones. The scan delay ten turn potentiometer on the front panel allows to minimize this delay in order to synchronize the whole system. The hierarchical behaviour of MIDAS is based on a 3-bit latch with its own priority encoder. It is always unabled at rest time, and represents the three flags for the three different MIDAS operations, previously referred.

#### 3.3.a) CONVERSION

The conversion is preceded by a waiting time for the conversion, depending on the timing diagram of the experiment. The waiting time for the conversion suspends the other two



operations, storing in a latch the last working address. So, at the end of the conversion, or -in case of no conversion- at the end of the waiting time, it is possible to continue the interrupted operation. The timing for the conversion is based, as previously seen, on the general 20 MHz clock and on the 8-step shift register, with a 400ns cycle. The first 200ns are used for reading the dark pedestal memory, the remaining for writing the results.

The conversion operation is made more complicated by the distance between the detector and MIDAS ubication.

In effect about 40 m of cables, to be covered in the two directions, are present between the two.

This means about 400 ns of delay between the starting of the command and the receiving of the data. Moreover to the delay due to the cables, it is necessary to add the delay introduced by the intrinsic operation mode of the flash ADC, corresponding to a clock cycle (400 ns).

To solve the problem introduced by the previously explained delays, we have introduced a phase difference of two steps (i.e.  $2 \times 400$  ns) working as coarse adjustment. The fine one is introduced using the scan delay ten turn potentiometer.

This phase difference involves the necessity to jump between two different memory addresses at each time: in fact while asking for the  $(n+2)$ -strip data, we are receiving the  $n$ -strip data.

In order to correct the offset, due to the Microplex (the same for all the 128 strips of the same chip), the following trick is used. The 8-bit flash ADC for the data conversion is used in order to allow the conversion of positive and negative values. In fact the zero corresponds to  $2^7$ , allowing to have, as converted extreme values  $\pm 128$ .

The operation begins with reading the converted data and storing them in the memory, also in case of overflow or underflow.

In order to simplify the explication we suppose to have only positive values.

Reading the datum for one channel, if different from zero, we subtract from it the value of a counter (at the beginning equal to zero). If the result is zero we read the next strip, if not, the counter is incremented of 1 (in case of negative values of -1) and only after we read the next strip. Once read the new

value, if different from zero we subtract from it the counter value. If the difference is positive we increment of 1 the counter value and so on up to the 128<sup>th</sup> strip. At this point the counter value is stored as mean value, to be used for the offset subtraction.

### 3.3.b) REREADING AND UPDATING

At the end of the conversion the latch bits are incremented in order that the next series of conversion will be registered in the following 1K channels. In order to increase the speed of all the system, usually the memory is not reset; simply the new data are overwritten on the existing ones. At the starting of the rereading, by means of a proper priority encoder, following the adopted philosophy the stored mean offset value is subtracted from the stored data and the results are written into the memory. Regarding the timing, the operation for each channel is developed in two 8-step cycles. In the first cycle is foreseen an eventual subtraction of the offset and in the second one the updating of the dark memory.

### 3.3.c) UPDATING AND TRANSMISSION

Depending on the proper flag value, automatically the transfer operation starts. Also in this case the addresses are memorized, to restart the interrupted operation at the same point. This operation is again executed in two 8-step cycles, plus the time needed for the handshake. In the first cycle, the converted data are read following the same modality of the first operation: but in this case the rewriting is inhibited to avoid an unrequired change in the memory contents. The end of this operation enables the transfer flag.

The second cycle begins with the flag reset and operates again the dark correction.

## 4) PERFORMANCE AND EXPERIMENTAL RESULTS

As usual, MIDAS was electronically tested to check the agreement with the design. Subsequently was successfully tested with

the special pulser DAG (17) and beta-sources to foresee its on beam behaviour.

Fig. 5 shows an event display collected using MIDAS having the input connected to DAG. The shaping of DAG is a gaussian leading edge for about  $1.5 \mu s$ , with a flat signal for about  $2 \mu s$  and a more sharp trailing edge for about  $400 ns$ . So each of the 39 pulses (each of different chosen height) has a proper not symmetrical width of about  $4 \mu s$ . Because the reading cycle of MIDAS has an own length of  $400 ns$ , a pulse of this width truly represents for MIDAS different pulses, as coming from 9-10 different strips which height corresponds to the instantaneous value of each single DAG pulse at the reading instant.

So the event display shape represents more or less the shaping of the DAG pulse, taking into account that each point (one "strip signal") corresponds to a  $400 ns$  width. Figs 6 represent the background of the electronic chain (driver box, Midas, detector, etc.) collected without (Fig. 6a) and with (Fig. 6b) pedestal and offset corrections.

Finally MIDAS was tested as electronic readout of one of the reference counters during the beam test of Delphi Microvertex Detector Prototype (18), in the CERN SPS North Area. The electronic set-up is shown in fig. 7. The system worked using a NMOS Microplex equipped  $25 \mu m$  DC-coupled detector (6) (256 channels with 2 VLSI readout chips). All the signals needed for chips and MIDAS were generated by the driver box.

The raw data collected were written on tape. Usually, as said at the beginning, the raw data in each channel consist of different contributions:

- 1) an overall dc-level (offset) common to all 128 channels of a single Microplex chip, multiplexed in one output. This varies from trigger to trigger and can be caused by external noise sources
- 2) a dark pedestal, reflecting fluctuations in channel characteristics across VLSI circuits and, as in our case of DC-coupled detectors, also contributions from the leakage current of each strip
- 3) the signal due to the collected charge as a result of the

passage of a minimum ionizing particle through the detector. The main advantage of MIDAS is to extract -ON LINE and in a very short time- from the previous different contributions only the one needed, i.e. the TRUE SIGNAL. This fact is clearly shown in following figures. Fig. 8 shows the pedestal distribution of MIDAS, that is on the level of 1 ADC count. In fig. 9 is represented the noise calculated for each 100 data, after the cutting out of bad channels. The mean value obtained is 2.8 ADC counts.

Fig. 10 shows an event display in sigma unit. The pulse-height on non fired strips is lower than 3 sigma. Finally the cluster pulse-height distribution for all the strips with pulse-height higher than 5 sigma was calculated, fig. 11, adding the signals from the two adjacent strips. A typical result for a 3-strip cluster is shown in fig. 12. As shown, the signal to noise ratio is about 18.

## 5) CONCLUSIONS

In conventional DC-coupled detectors the flow of leakage current to the input stage causes baseline variations among the readout channels requiring large dynamics ADCs. Moreover the Microplex introduces, as previously seen, sudden variations of the offset for all the channels. MIDAS, designed to overcome these difficulties, is able to process up to 1024 channels at 2.5 MHz readout speed with an accuracy of 8-bit, completing on-line the pedestal and offset analog subtraction and giving results with a signal to noise ratio for a m.i.p., that is in good agreement with the results obtained with different detectors, but using equivalent Microplex, so allowing to achieve an expected resolution of about 5  $\mu\text{m}$ .

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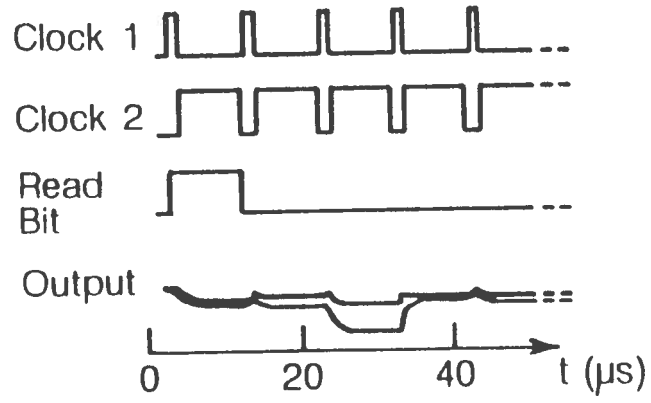


Fig. 1 - Control and output signals during readout

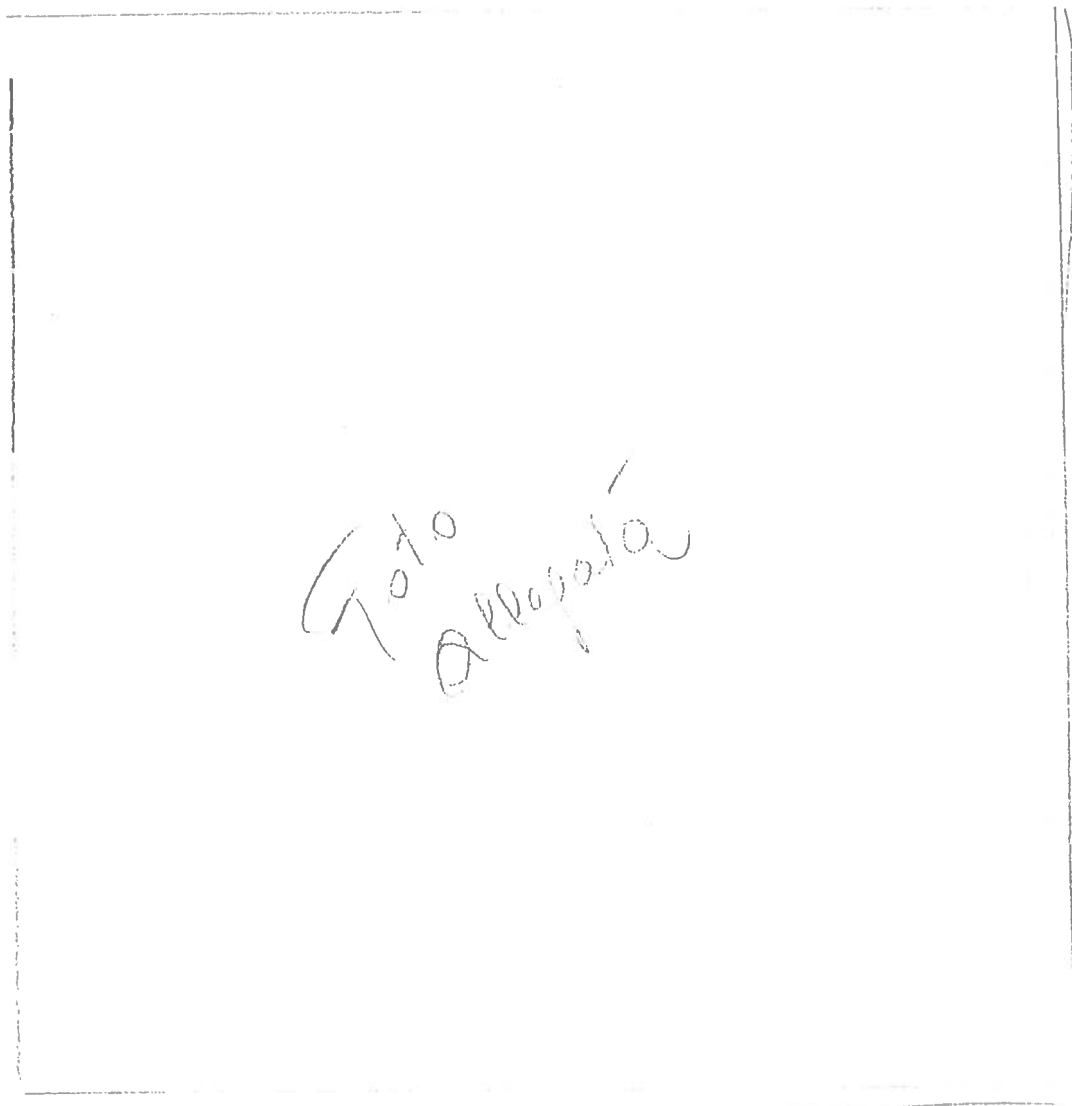


Fig. 2 - The front panel

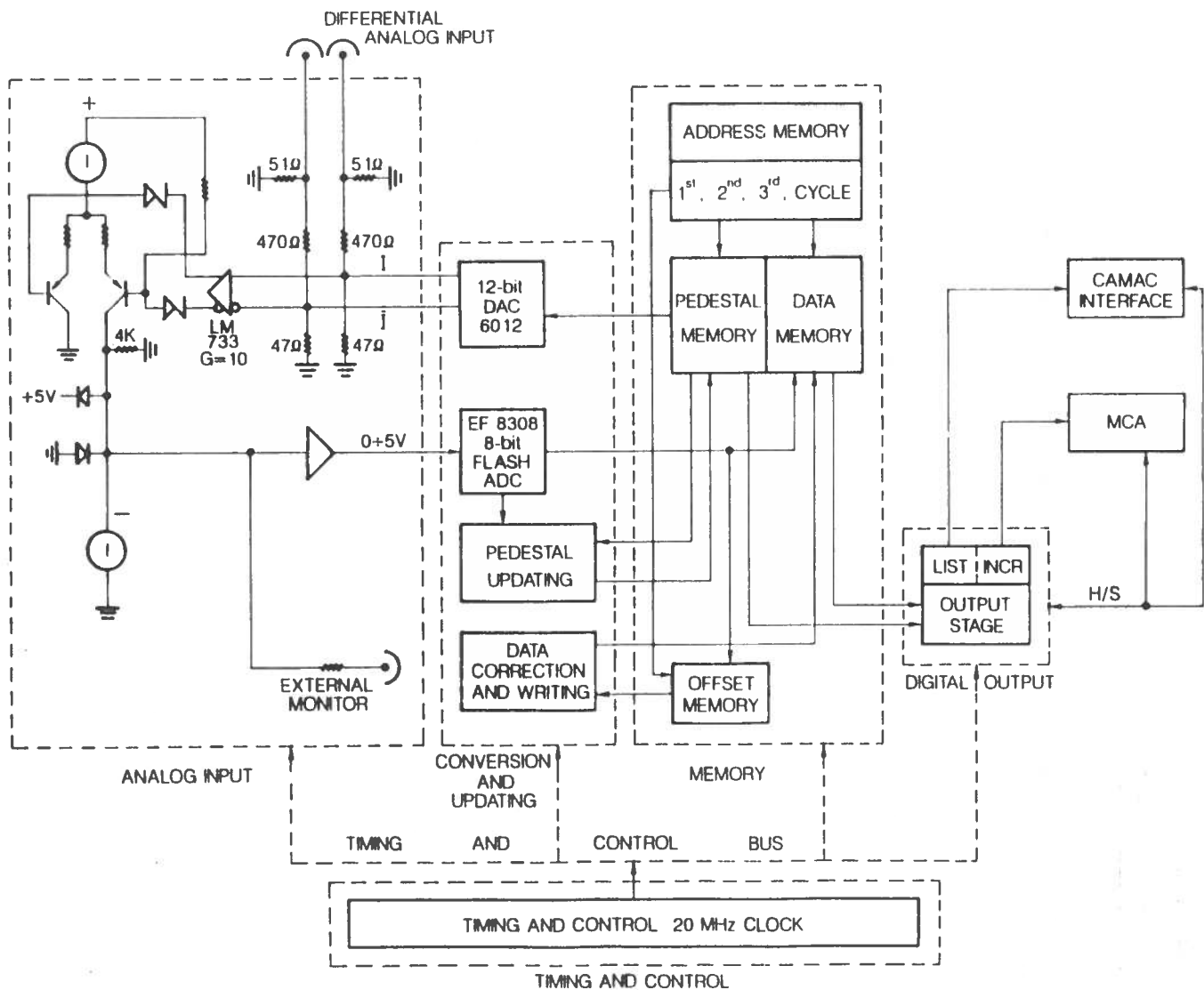


Fig. 3 - General schematic

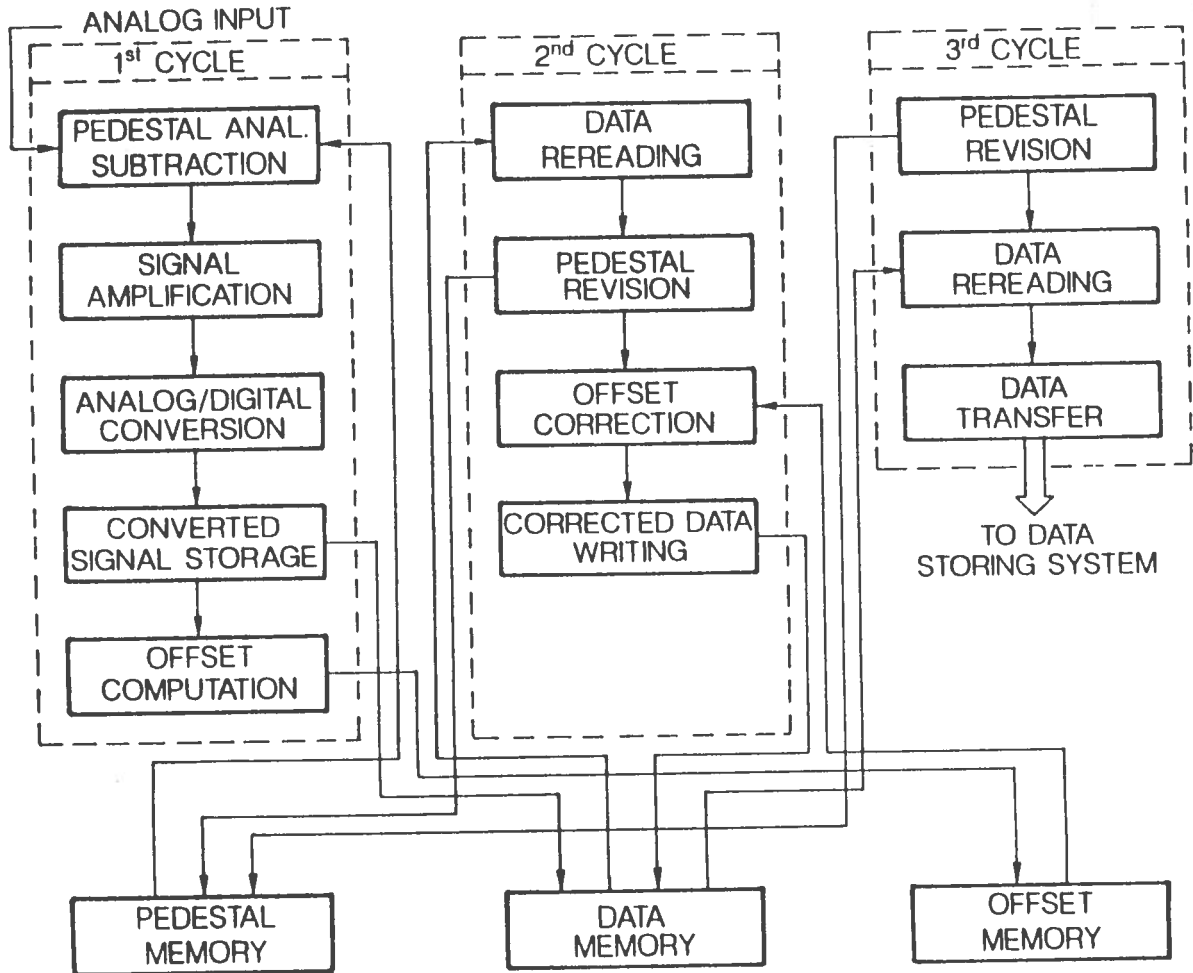


Fig. 4 - Working mode simplified block diagram



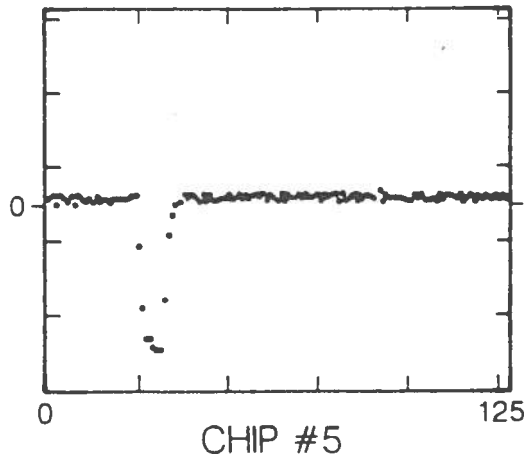


Fig. 5 - Event display with the DAG generator

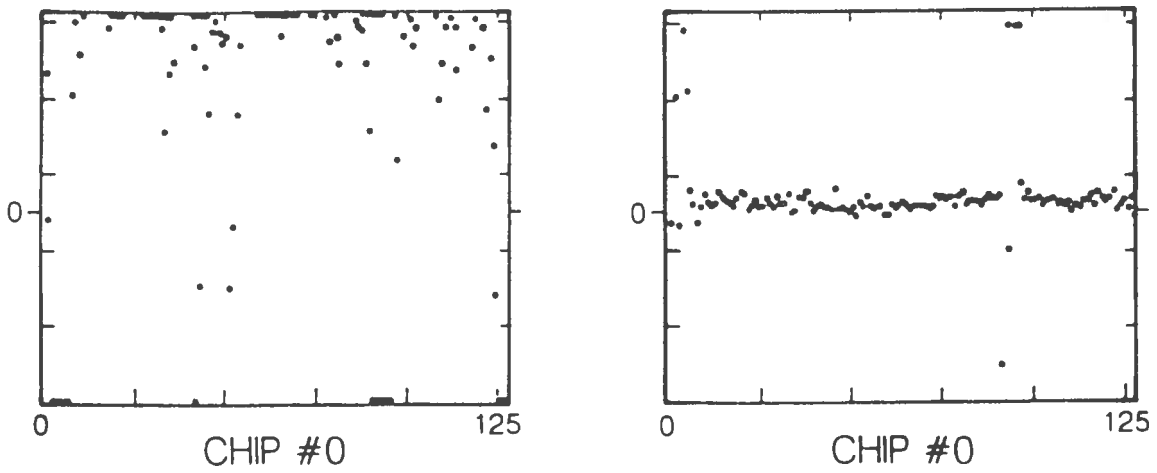


Fig. 6 - Detector background without (a) and with (b) pedestal and offset correction

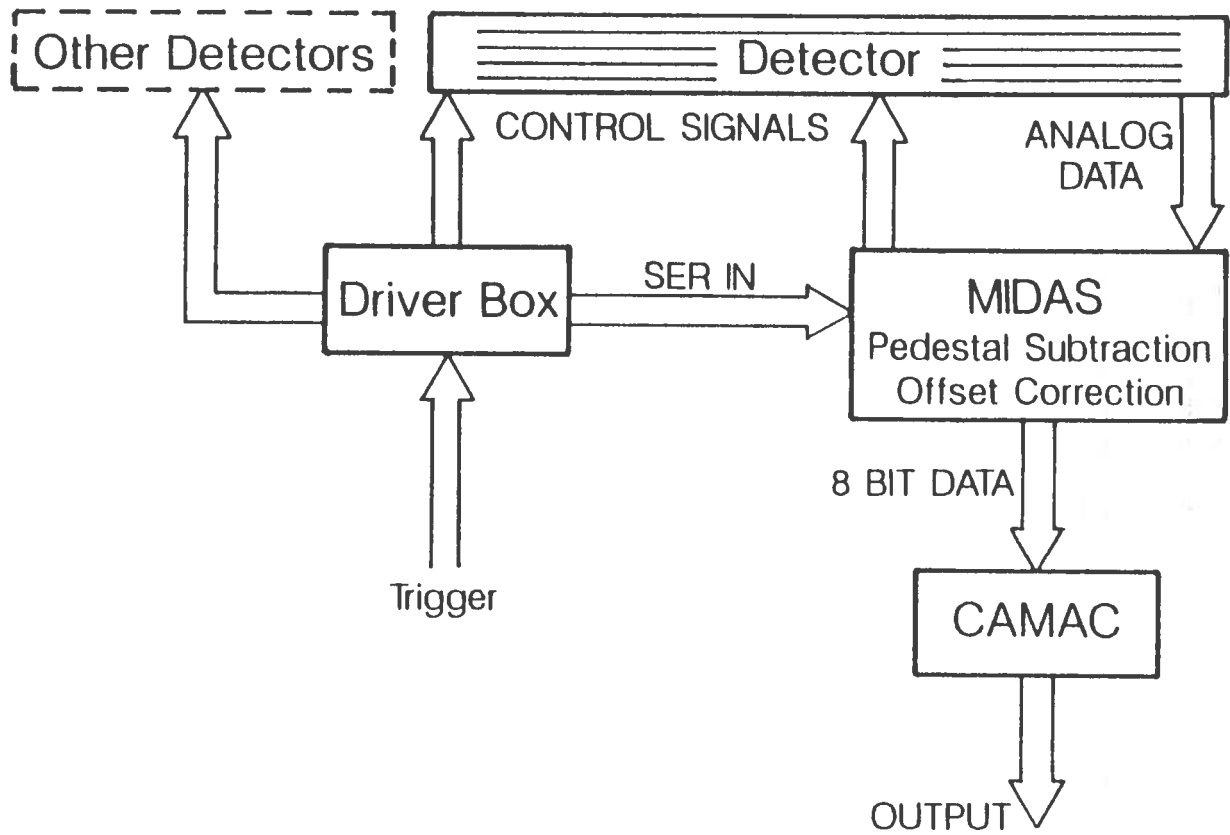


Fig. 7 - Schematic view of set-up during the beam test

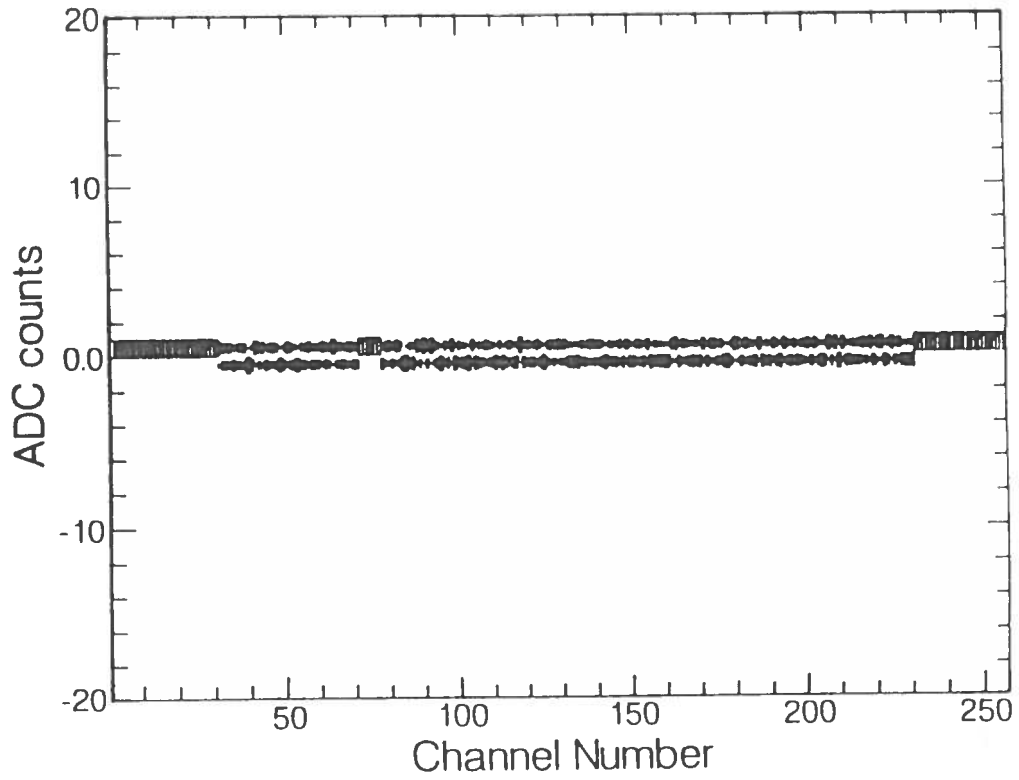


Fig. 8 - Pedestal distribution calculated for each channel

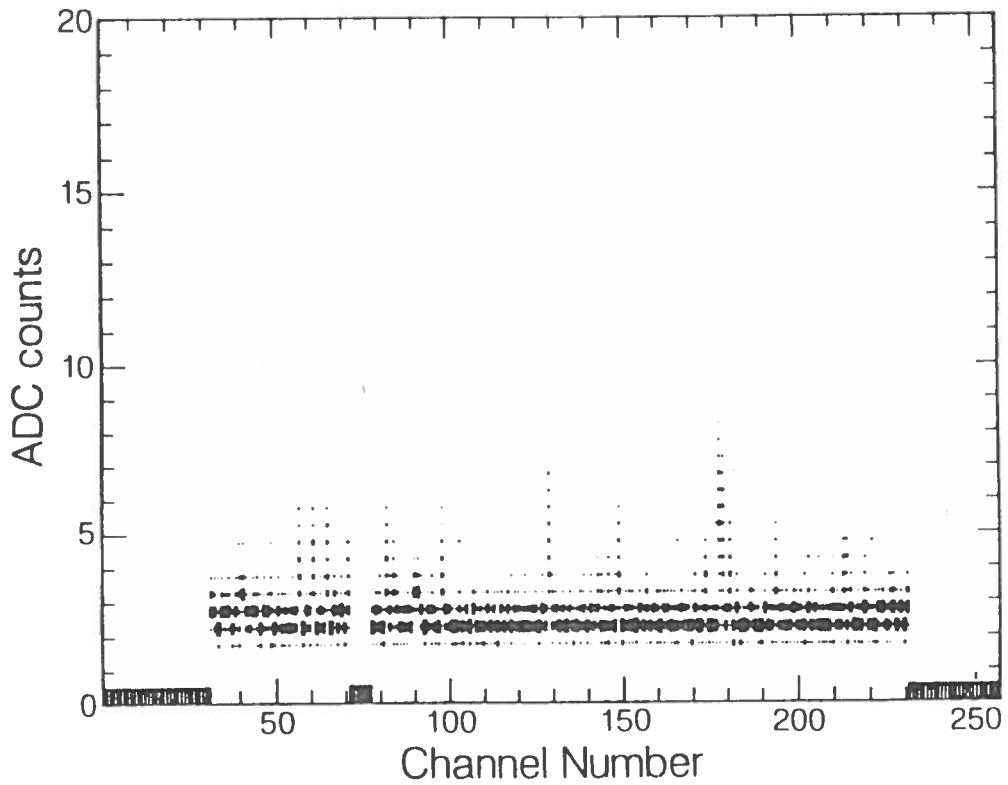


Fig. 9 - Noise distribution calculated for each channel

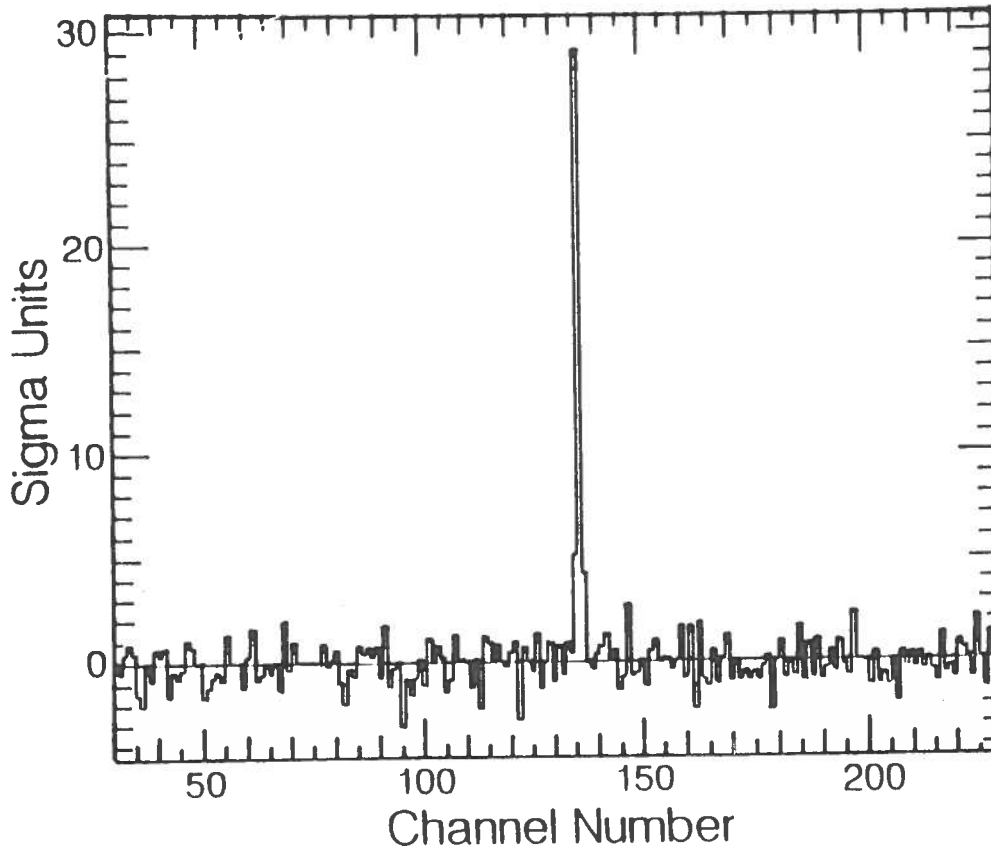


Fig. 10 - Event display

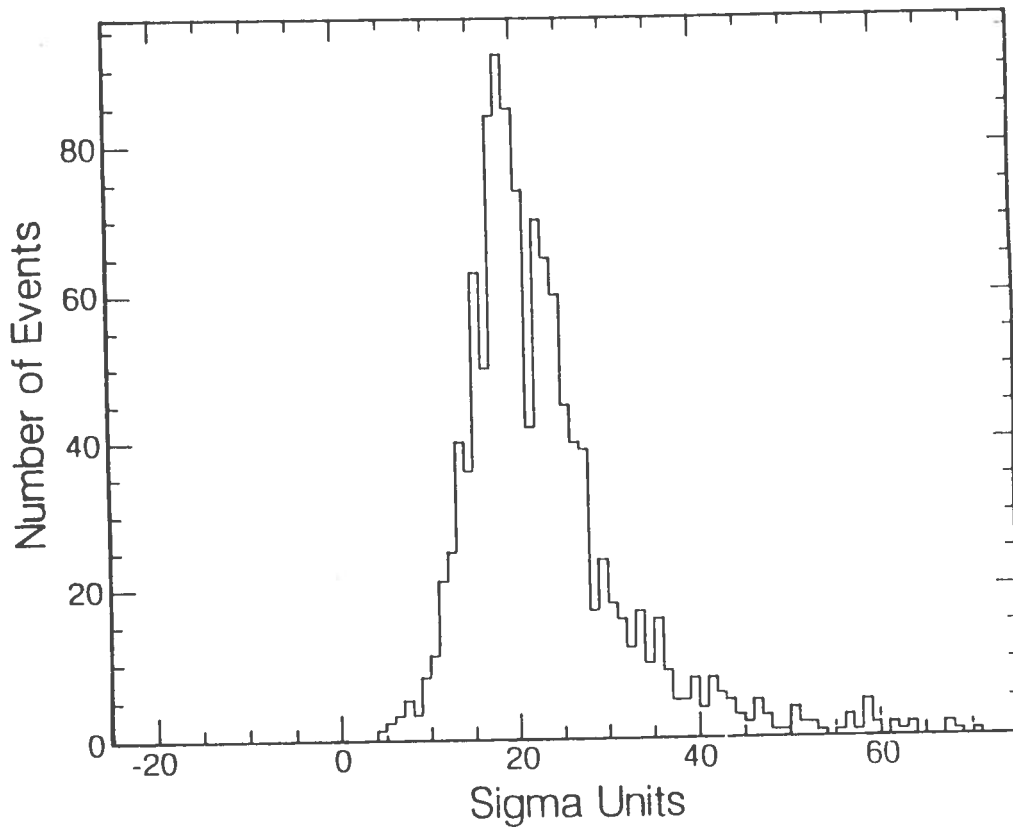


Fig. 11 - Cluster pulse height distribution

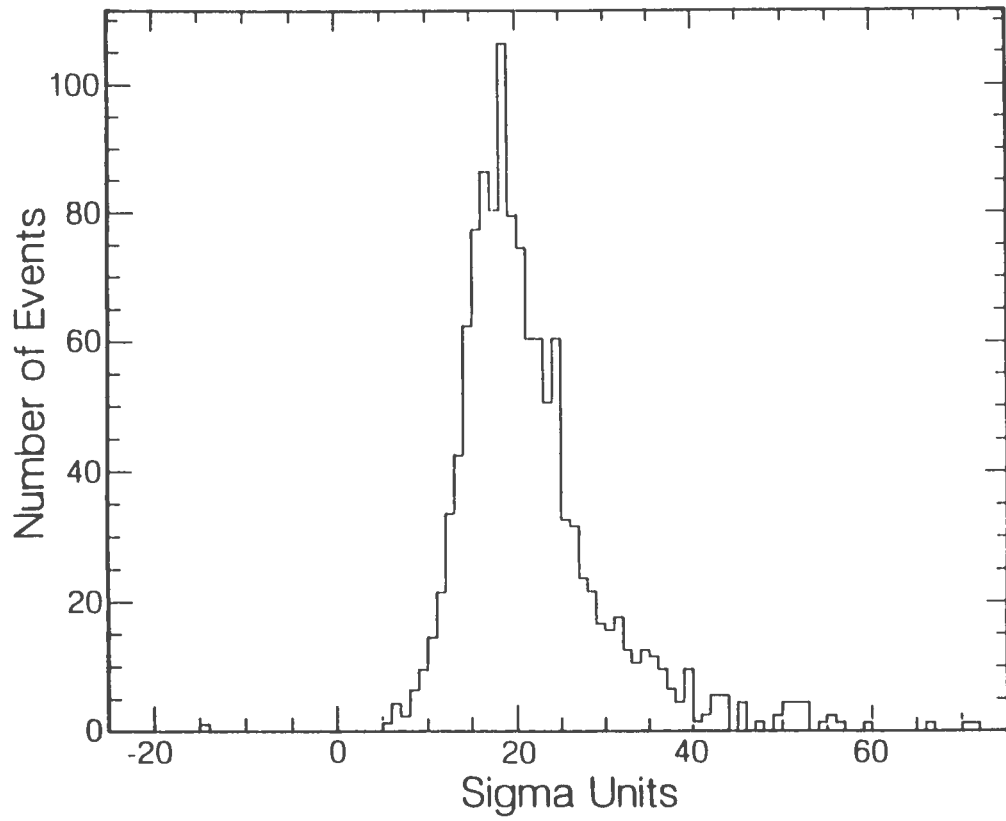


Fig. 12 - 3-strip cluster pulse-height distribution