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THE TEST SYSTEM OF THE DIGITAL ELECTRONICS FOR THE CHARM II LIMITED STREAMER TUBES

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abstract:

We describe the system presently used to perform the large scale quality control of the front-end digital electronics developed by the CHARM II collaboration for fast read-out of limited streamer tubes. The system is capable of localizing individual defective components and faults in the layout. A detailed list of trouble shooting procedures is given in the Appendix.

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1. INTRODUCTION

A new calorimetric detector is being set-up by the CHARM II collaboration for a precise measurement of the electroweak mixing angle in the purely leptonic reaction $\nu_\mu e \rightarrow \nu_\mu e$ [1]. The active element of the detector, being installed on the CERN SPS neutrino beam line, consists of a system of about 150 thousand limited streamer tubes [2]. Both the digital information of the tube wire and the analog information of external pick-up strips, used for precise definition of the shower position and energy, are read-out.

The operation of streamer tubes at a fixed target experiment such as CHARM II, with event rates during the burst up to about 100 Hz, demanded the development of a read-out electronics [3] significantly different from commercially available products. The shaper cards of the digital electronics accomplish two functions. First they produce a fast signal for the trigger logic (Σg) from the streamer pulses; then, if strobed by the return of a trigger, they store the status of the streamer wires in latches which are fully read-out in about 1 μs into memory buffers.

The streamer tubes are arranged in 420 planes of 352 tubes, built in 44 groups of 8 tubes per plane. Each shaper card serves 32 wires, so that 11 cards are needed to equip a plane, for a total of 4620 cards. Due to the large scale of the system, we also had to develop a dedicated test device capable (before installation and later) of probing on the bench all the functions of a shaper card. We aimed at the design of a system capable of a localized diagnosis of faults in the layout and of defective components.

2. THE SHAPER CARD

A simplified block diagram of the shaper card is drawn in Fig.1. Eight MC3430 provide 32 comparators serving the streamer tube signals arriving on the central connector. Each comparator acts both as discriminator and as monostable producing a 400 ns positive TTL output. The 32 outputs are fed to the logic producing the Σg signal and to a 32 bit multiplexer/latch.

The Σg circuitry consists of 8 quad SN74LS126 and 4 summing resistors. The Σg signal is a sum of groups signal, a single valued function of the number (≤ 44) of "groups of 8" tubes in the plane with at least one hit. It is used to construct the first level trigger, and also enters a second level trigger performing the separation of electron showers (small Σg) from hadronic showers (large Σg). It is formed from the comparator outputs which are fed to the "enable" of 32 three-state buffers (SN74LS126) having the inputs grounded and the outputs connected together in groups of 8, in a quasi wired-OR mode. The 4 "groups of 8" so obtained are connected together through four 681 Ω resistors. The Σg signals from the 11 cards, serving an entire plane, are then ORed together on a main bus. The far end of this bus line is connected to the power supply through an additional resistor so that a global Σg analog signal is available to the trigger decision fast logic.

The 11 cards serving one plane are daisy-chained in a shift register-type connection; the 32 bit mux/latch of each card, consisting of a 8 SN74LS298

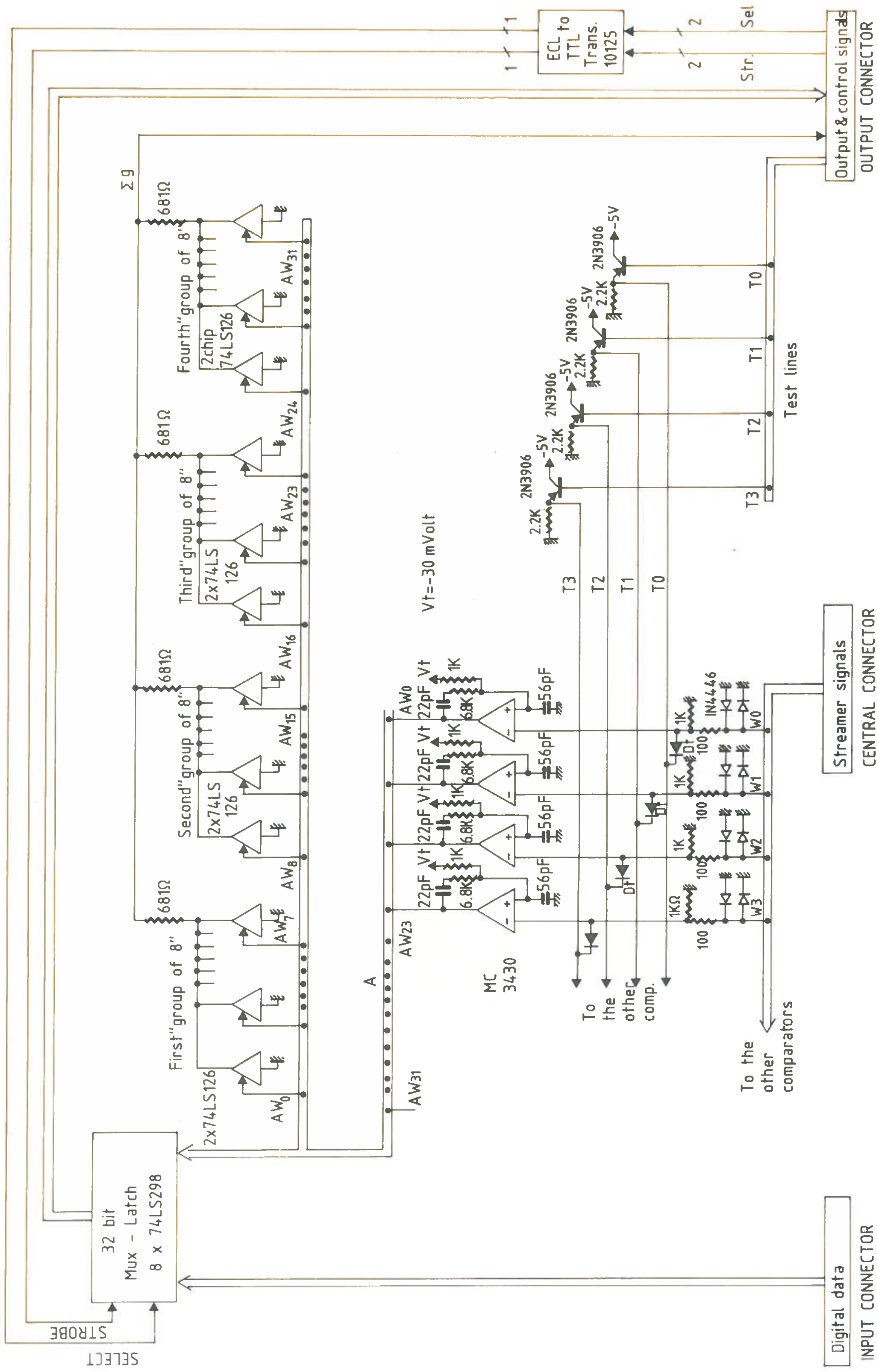

FIG. 1 SHAPER CARD BLOCK DIAGRAM

chips, can receive data either from the comparators or, alternatively, from the latch of the previous card, via an output and an input connector. The status of the 32 comparators is latched at the time of a STROBE signal 350 ns after the occurrence of a triggering event. Then a SELECT control signal enables input from the previous card and 11 additional STROBEs, spaced by about 100 ns, transfer the content of the latch of one card into the latch of the next until the eleven 32 bit words are stored in a memory buffer.

In addition, 4 test lines T_0,T_1,T_2 and T_3 are built into the card to allow for the on-line monitoring of its integrity. Each test line T_i (i=0,3) is designed to pulse 8 equally spaced comparators (i+4l, l=0,1,2,...7).

3. THE TEST PROCEDURE

The front panel of the test box is shown in Fig.2. The shaper card under test is held by mechanical guides and is connected to the test box circuitry through its standard three 64-pins Harting connectors.

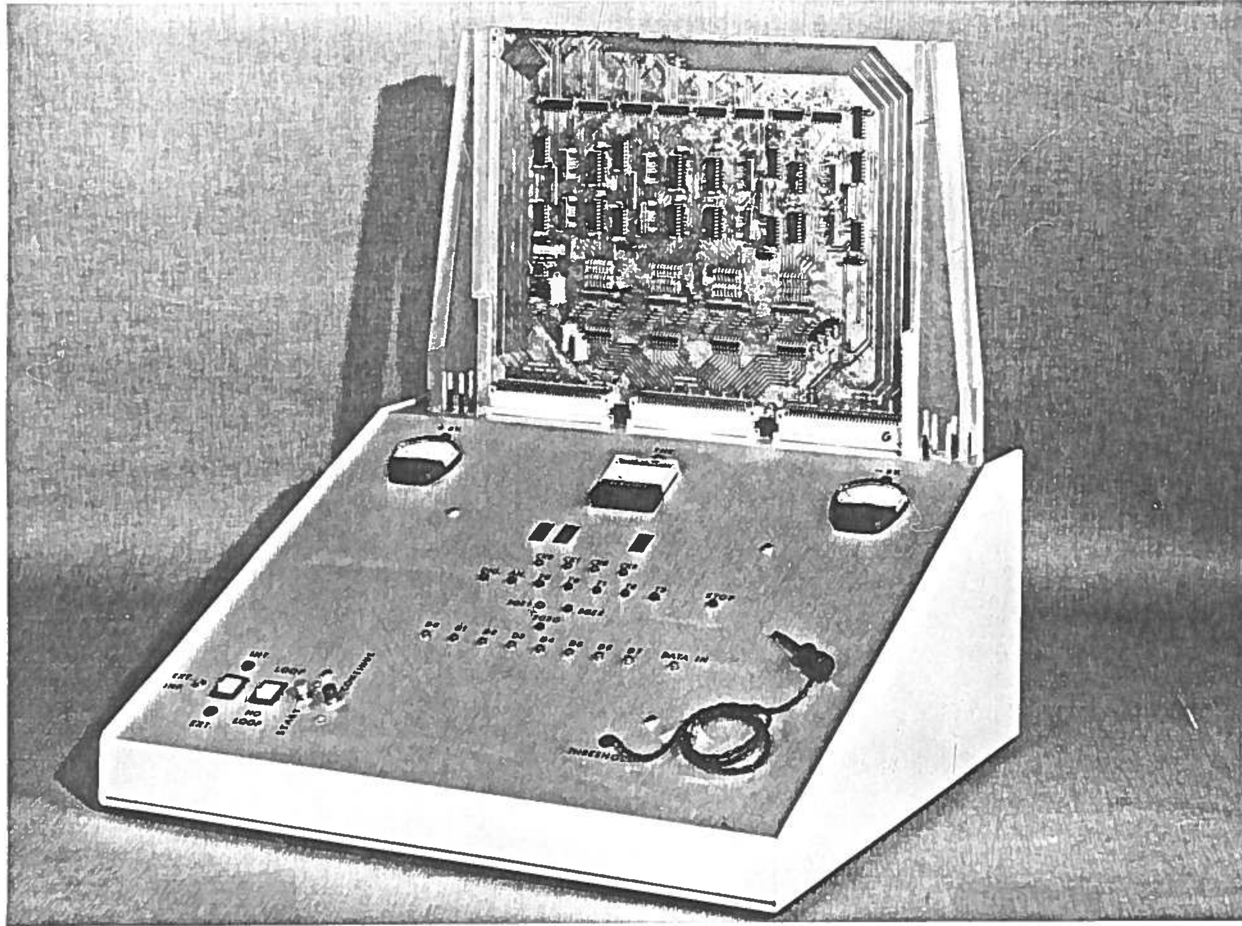

Fig. 2 - Test box front panel

The basic timing of events during the test procedure is provided by four phase clocks CK_0,CK_1,CK_2 and CK_3. They are monitored by four LED's on the front panel, and are all derived (Fig.3) from a common master clock, enabled via the START button.

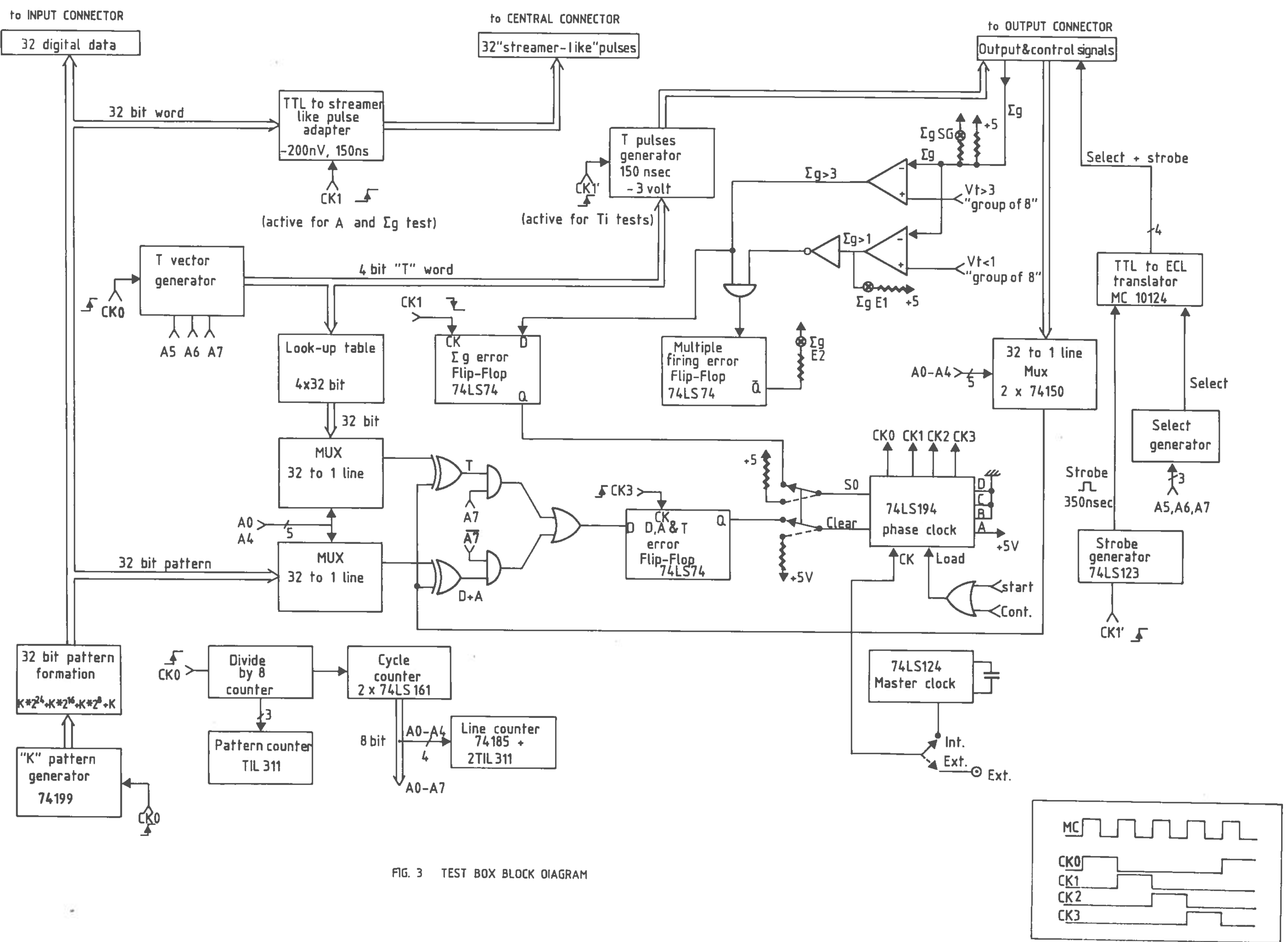

FIG. 3 TEST BOX BLOCK DIAGRAM

The complete procedure consists of 256 cycles, split among successive tests of seven different data paths on the shaper card. They are, respectively, the digital D data path (32 lines from the input to the output connector through the mux/latch), the analog A data path (32 lines from the central to the output connector through comparators and mux/latches), the Σg data path (one single analog output from the 32 input lines on the central connector) and the test lines T_0,T_1,T_2 and T_3 data paths. Each of the 256 cycles consists of a set of elementary write and read operations (Table 1).

Table 1

cycle	test	# of elementary operation/cycle	# of elementary operations	A5 A6 A7
1-32	D	8	256	0 0 0
33-64	A	8	256	1 0 0
65	Σg	8	8	0 1 0
66-128	dummy	-	-	any 1 0
129-160	T_0	1	32	0 0 1
161-192	T_1	1	32	1 0 1
193-224	T_2	1	32	0 1 1
224-256	T_3	1	32	1 1 1

An elementary operation consists of the input of a known pattern into one of the above paths (on the leading edge of the clock signal CK_0 or CK_1) and its comparison with the pattern read-out on output (at the time CK_3, except for Σg where a delayed CK_1 is used).

Sufficient information and redundancy for the D,A and Σg tests is obtained using only eight 32-bit input test patterns, each containing 4 "ones" and 28 "zeros". They have the general form:

$$K*2^{24} + K*2^{16} + K*2^{8} + K \qquad (1)$$

where K is an 8-bit word containing a "one" and seven "zeros". These 8 patterns are input in the form of TTL data for the D test, thus simulating data transfer from the previous card, and in the form of 200 mV negative pulses, 150 ns wide, for the A and Σg test, thus simulating the arrival of streamer pulses. The test lines data paths are tested by successively firing them, one by one. The shaper card itself then produces , at the comparator inputs, a 32 bit pattern of 8 equally spaced "ones" and 24 "zeros" (Fig.1). The D,A and T_i tests demand successful comparison, line by line, of the input and output patterns. The Σg test demands the detection of a Σg output level equivalent to four "groups of 8" having at least one hit.

Through its 256 cycles, the procedure tests good operation of each line and absence of cross-talk among them. If failures are detected, the procedure halts, displaying diagnostic information by means of a syntax code of the type (j-nn-k)

available on the front panel: j is one of the seven front panel LED's ($A, D, \Sigma g, T_0, T_1, T_2, T_3$) indicating the data path being tested, nn is a two digit line counter, displaying the line (1-32) under test, k is a one digit pattern counter displaying the bit position (0-7) set to "one" in the eight bit word K defined above; the bits of the word K are also displayed by eight front panel DATA LED's. The syntax code thus guides diagnostics and trouble shooting.

Three additional errors can be detected on the Σg path and displayed on dedicated front panel LED's. They indicate respectively multiple firing of one or more comparators (Σg E1), a group of eight steady to "one" (Σg E2) and a short to ground anywhere along the Σg line (Σg SG).

Two front panel instruments are used to measure the currents flowing on the negative and positive power supplies. The third meter measures the bias voltage V_{bias} of the MC3430 chips which fixes the effective threshold for pulses from the streamer tubes.

The test can be performed either at the fixed speed of the internal clock or, by means of the EXT switch, at variable speed using a pulse generator as an external clock. In the normal mode of operation (NO-LOOP) the test box halts on detection of a failure. It proceeds by pushing the CONTINUE button and may stop again in case of additional failures. It finally stops at the end of the test (STOP LED on).

If the LOOP switch is active, instead, all halt features are disabled and the system will loop over its 7 phases unless externally stopped. The use of an external clock is a very effective way of looping on errors at any desired frequency, thus allowing careful investigation of failures. The use of the external clock in single-step mode also proved very useful for trouble shooting.

4. HARDWARE IMPLEMENTATION

A block diagram of the test circuitry is shown in Fig.3. Its main components are:

a) the master clock: this is produced either by a SN74LS124 or by an external data pulser and is fed directly to the clock input of a SN74LS194 shift register. Pushing the START button enables, through the parallel loading of the pattern "1000" into the SN74LS194, via its S_1 control pin, the generation of the 4 phase clocks CK_0, CK_1, CK_2, CK_3 (Fig.3) governing the timing of the operations performed by the system.

b) The pattern generator: this is a SN74199 shift register whose function is to output, on the leading edge of CK_0, a different 8-bit word K, with only one bit set, according to prescription (1). The pattern generator drives the 8 front panel data LED's. A TIL3111, acting as a one digit pattern counter, displays on the front panel the bit number set to one in the word K. A complete loop of the pattern generator over its eight states constitutes a cycle of the procedure.

c) The cycle counter: built with two SN74LS161, it contains the number n (n=1,256) of the cycle currently being executed and is incremented by each 8-th CK_0 pulse. The $D, A, \Sigma g, T_0, T_1, T_2, T_3$ tests are activated respectively for $\overline{A5}*\overline{A6}*\overline{A7}=1$, $A5*\overline{A6}*\overline{A7}=1$, $A6*\overline{A7}=1$, $\overline{A5}*\overline{A6}*A7=1$, $A5*\overline{A6}*A7=1$, $\overline{A5}*A6*A7=1$, $A5*A6*A7=1$

(see Table 1), where A0 through A7 are the 8 bits of the cycle counter. These products, fed to open collector buffers, also drive the corresponding front panel LED's. Bits A0 through A4 contain the number of the line currently being tested and drive, via a 74185 decoder, the two TIL311 displays acting as a two digit line counter on the front panel.

d) The strobe generator: this is built with a SN74LS123 monostable triggered by the leading edge of CK_1. Ck_1 is a clock derived and timed by CK_1 but properly gated by the various A5*A6*A7 products to suit the needs of the different phases of the procedure. Whenever the 350 ns output of the SN74LS123 is present, its trailing edge simulates the arrival of a STROBE to the mux/latch of the shaper card.

e) The select generator: it provides the control signal necessary to enable storage in the mux/latch of data from the input connector at the beginning of the procedure and then storage of data from the 32 analog lines at the beginning of the A test for the remainder of the procedure.

The 256 cycles of the full test procedure, timed by 2048 CK_0 pulses, can be completed in a fraction of a second. The system is protected against shorts to ground: TTL outputs are all open collector and the analog outputs all come from current sources.

The first 32 cycles constitute the D test, each cycle testing one of the 32 data lines. The pattern generator loops over its eight patterns and the correctness of the response of the line under test is checked 8 times. Two selection multiplexers, each made by two SN74150 chips and driven by lines A0 through A4 of the cycle counter, select for comparison the same i-th line (i=1,32) respectively from the input and output pattern. The comparison is made by an exclusive OR SN74LS86, and the result of the comparison is stored in a SN74LS74 error flip-flop on the leading edge of CK_3.

During the following 32 cycles, constituting the A test, the same sequence of events takes place, the only difference being the conversion of the TTL data from the pattern generator to 150 ns, 200 mV negative "streamer-like" pulses on the leading edge of CK_1. The timing of the simulated STROBE is then appropriate to check proper operation of the MC3430 as a monostable of 400 ns.

The 65-th cycle performs the Σg test. The Σg output is compared eight times, through an MC3430 comparator, to a level corresponding to more than 3 "groups of 8" having at least one hit. The result of the comparison is latched in an additional SN74LS74 flip-flop 350 ns after the CK_1 leading edge.

The Σg output is also compared against a level corresponding to one "group of 8" having at least one hit. The presence of a $\Sigma g > 1$ response in anticoincidence with $\Sigma g > 3$, indicative of multiple firing of one or more comparators, lits the $\Sigma g\ E_1$ front panel LED.

The d.c. presence of a $\Sigma g > 1$ response signals on the Σg E2 front panel LED, that one or more "group of 8" is steadily drawing current. An additional Σg SG LED signals a short to ground anywhere along the Σg bus line. The last two error conditions are immediately detectable as soon as the test system and the shaper card are powered. After the Σg test, CK_1, is inhibited for the duration of 63 cycles. No action takes places.

The T_0, T_1, T_2, T_3 tests follow, each lasting 32 cycles. The test line T_i to be

pulsed (i=0,3) is selected by the bits A5 and A6 of the cycle counter. All except the first of the 256 CK_1 pulses contained in the 32 cycles are inhibited. On the leading edge of this unique CK_1 pulse, the line T_i is pulsed with a 150 ns, 3 V negative pulse; 350 ns later, the corresponding unique STROBE latches the status of the MC3430's of the shaper card. The 32 cycles of the T_i test check the output lines one by one, while the 32 comparators stay idle. Line selection and comparison proceeds via a duplicate of the multiplexer and exclusive OR sequence used for the D and A test. Error conditions are latched by the same SN74LS74 flip-flop.

When an error (mismatch) condition is detected on the error flip-flop shared by the D,A and T_i tests a CLEAR is sent to the SN74LS194 shift register. Similarly, when an $\Sigma g < 3$ response causes a transition of the Σg error flip-flop, the S_0 control line of the SN74LS194 is pulled low. In both cases, further clock generation is inhibited. Unless in loop mode, the system halts.

The cycle counter and the pattern generator are never reset; the relevant syntax code is thus displayed for the duration of the halt. A push on the CONTINUE button resumes the test from the point of the interruption by loading the SN74LS194 again and clearing the error flip-flop.

The action of the front panel LOOP/NO-LOOP switch consists of the opening of the CLEAR and S_0 lines, the two lines being pulled to a high level through two resistors, disabling the halt features.

5. EXPERIENCE WITH THE SYSTEM

The test system effectiveness was first examined by purposely inducing faults on a few shaper cards. The system proved capable of recognizing all the faults we were able to think of. Many faults turn out to be expecially easy to diagnose because of the simultaneous detection of several error syntax codes. In the vast majority of cases an immediate detection of the faulty component or connection is provided. A complete discussion of the diagnostic and trouble shooting procedure is contained in the Appendix.

Real life experience with the system is now being rapidly acquired. The test procedure proved very useful in testing a first limited pre-series of shaper cards to be used on prototype streamer tubes. Several test boxes have been built by now. Some of them, made available to the manufacturer company of the shaper cards, are presently coping successfully with their basic task of quality control of the mass production process.

Acknowledgements

We wish to thank D.De Pedis and J.Schuett for very valuable discussions in the design phase and A.Candela, F.Manna, L.Parascandolo and A.Perricone, for their contribution to the realization of the system.

REFERENCES

[1] CHARM II proposal CERN/SPSC/83-24 and addendum CERN/SPSC/83-37.
[2] G.Battistoni et al., Nucl. Instr. and Meth., 164 (1979) 57.
[3] The digital electronics of the CHARM II streamer tube system will be described in a forthcoming publication.

APPENDIX

The reader should make reference to Fig.3 and to the details of Fig.4a, 4b, 4c and 4d.Fig.5a, 5b, 5c containing the connector pin-out for the shaper card.

Digital data path.

If the test system detects an error in the digital path this can depend on the following possible causes:
1) Bad soldering on the digital input connector.
2) Interrupted connection between the digital input connector and the mux SN74LS298 chip.
3) Short to ground before the SN74LS298.
4) Short between two adjacent lines.
5) Defective SN74LS298.
6) Failure in the select to the SN74LS298.
7) Failure in the clock to the SN74LS298.
8) Groundless SN74LS298.
9) Unpowered SN74LS298.
10) Output of the SN74LS298 shorted to ground.
11) False or interrupted connection between the SN74LS298 and output connector.
12) False soldering on the output connector.

We now analyze how to take action against these problems:

1) The detection of a cold soldering is a very difficult task because it can give intermittent problems. If a cold soldering is suspected, it is better to solder all the points connected to the line again (on the input connector, on the chip, and on the output connector).
2) This is detected very easily by the test-box. It gives the number of the interrupted line.
3) Same as above. The test box sees always a "zero".
4) The test box stops twice: on the first shorted line and on the adjacent one.
5) There can be either a false soldering on the chip or a partially (or totally) faulty chip.
6) If there is no select to the SN74LS298 chip, then we have four defective lines.
7) Same as above. It can apply to a single or more chips.
8) In this case the zero level rises to about 1 Volt, depending on the chip.
9) The test box stops four times in the digital, four times during the analog test and in T_0,T_1,T_2,T_3 test.
10) In this case the test box stops both on digital and analog.
11) The test box stops in digital and analog tests. It is better to solder all the pertinent points again.
12) Same as above.

Analog path

If the test box detects an error in the analog path, this may depend on the following:
1) False soldering on the central connector.
2) False soldering on the series resistor R1.
3) Series resistor too large.

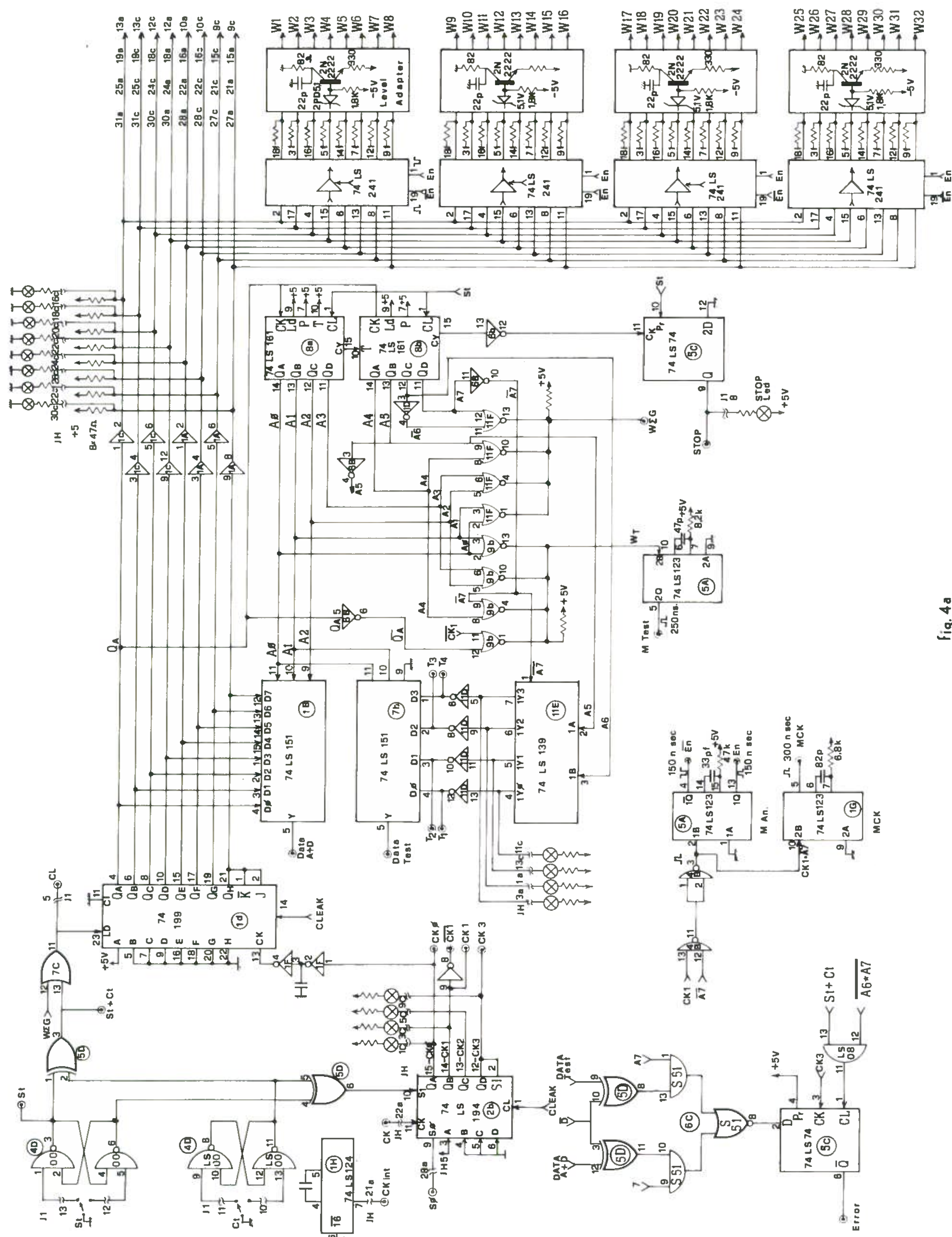

fig. 4a

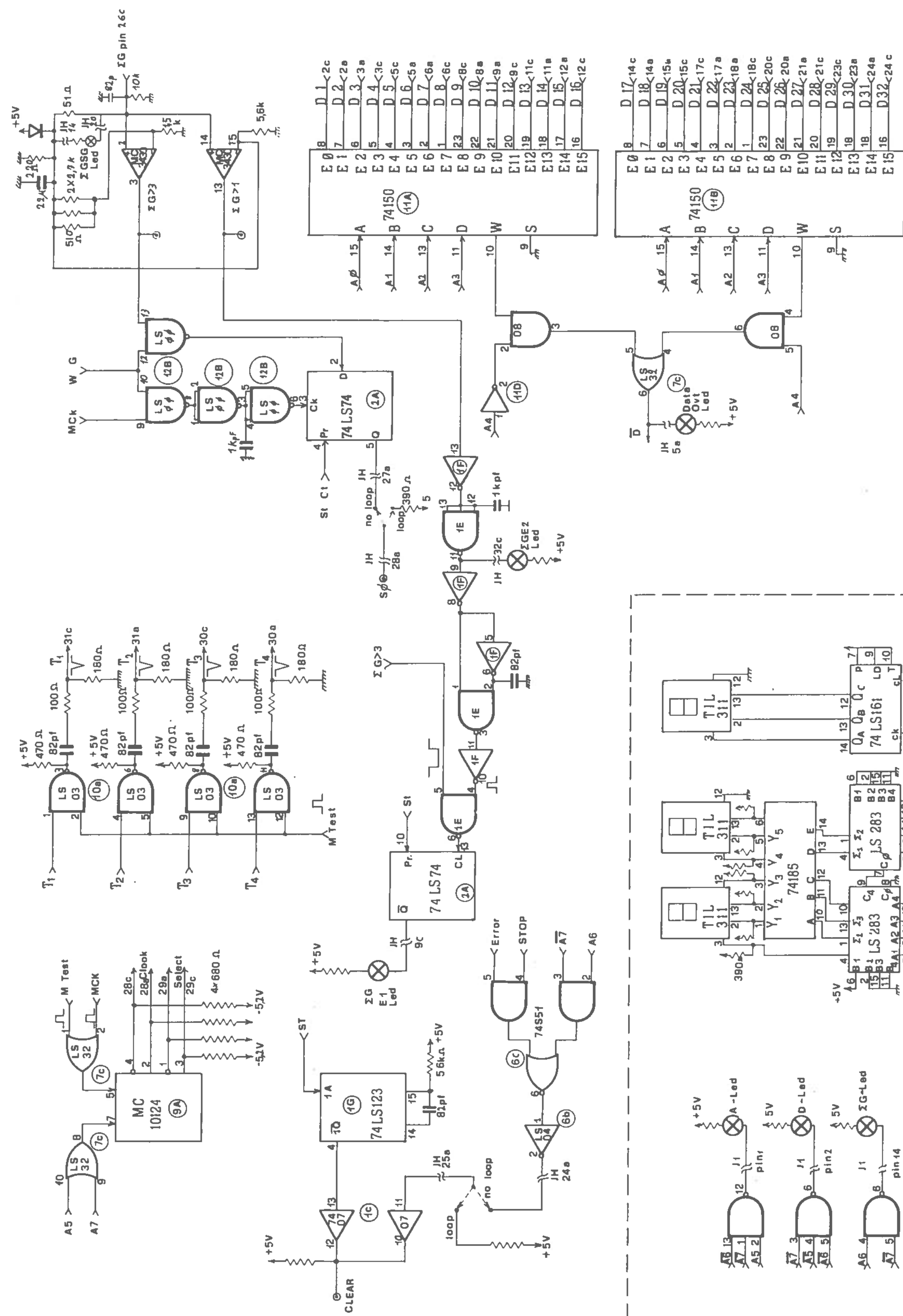

fig. 4b

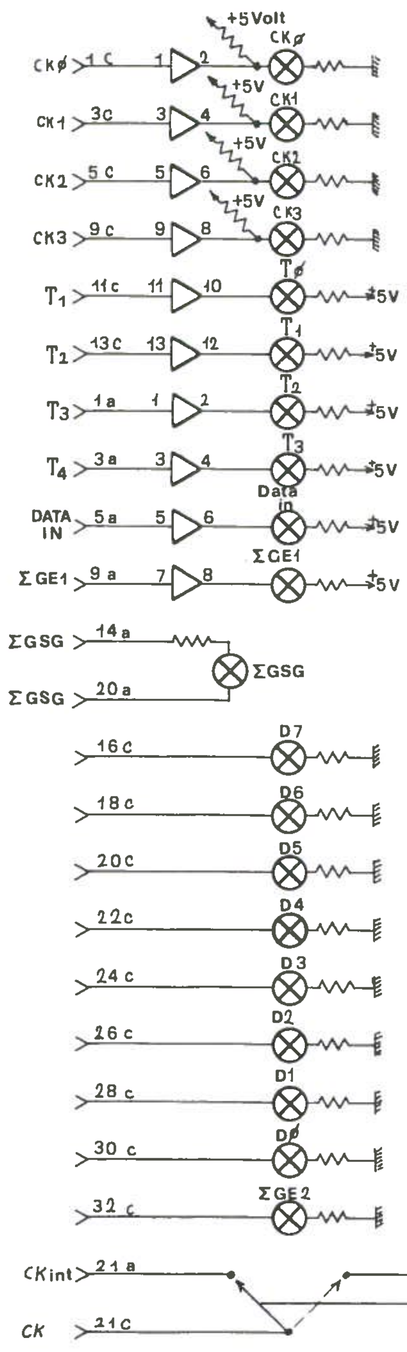

fig. 4c

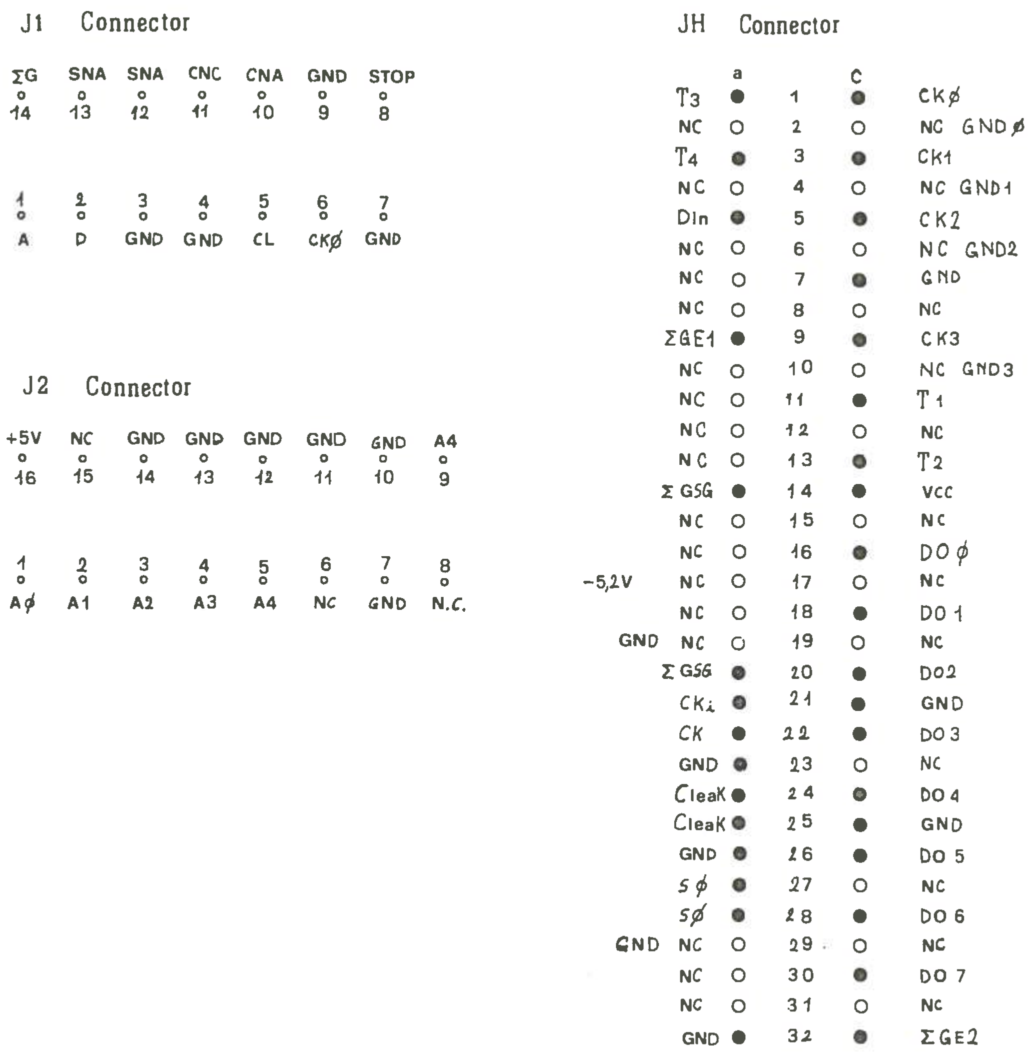

fig. 4d

SHAPER CARD INPUT CONNECTOR

WIRE	INPUT		SIGNALS
WIRE-SIG	32	c 1 a	GND
WIRE-SIG	31	c 2 a	GND
WIRE-SIG	30	c 3 a	GND
WIRE-SIG	29	c 4 a	GND
WIRE-SIG	28	c 5 a	GND
WIRE-SIG	27	c 6 a	GND
WIRE-SIG	26	c 7 a	GND
WIRE-SIG	25	c 8 a	GND
WIRE-SIG	24	c 9 a	GND
WIRE-SIG	23	c 10 a	GND
WIRE-SIG	22	c 11 a	GND
WIRE-SIG	21	c 12 a	GND
WIRE-SIG	20	c 13 a	GND
WIRE-SIG	19	c 14 a	GND
WIRE-SIG	18	c 15 a	GND
WIRE-SIG	17	c 16 a	GND
WIRE-SIG	16	c 17 a	GND
WIRE-SIG	15	c 18 a	GND
WIRE-SIG	14	c 19 a	GND
WIRE-SIG	13	c 20 a	GND
WIRE-SIG	12	c 21 a	GND
WIRE-SIG	11	c 22 a	GND
WIRE-SIG	10	c 23 a	GND
WIRE-SIG	9	c 24 a	GND
WIRE-SIG	8	c 25 a	GND
WIRE-SIG	7	c 26 a	GND
WIRE-SIG	6	c 27 a	GND
WIRE-SIG	5	c 28 a	GND
WIRE-SIG	4	c 29 a	GND
WIRE-SIG	3	c 30 a	GND
WIRE-SIG	2	c 31 a	GND
WIRE-SIG	1	c 32 a	GND

Fig.5a

SHAPER CARD OUTPUT CONNECTOR
DIGITAL
CONTROL & DATA OUTPUT

c	pin	a
GND	c 1 a	GND
D01	c 2 a	D02
D04	c 3 a	D03
GND	c 4 a	GND
D05	c 5 a	D06
D08	c 6 a	D07
GND	c 7 a	GND
D09	c 8 a	D10
D12	c 9 a	D11
GND	c 10 a	GND
D13	c 11 a	D14
D16	c 12 a	D15
GND	c 13 a	GND
D17	c 14 a	D18
D20	c 15 a	D19
GND	c 16 a	GND
D21	c 17 a	D22
D24	c 18 a	D23
GND	c 19 a	GND
D25	c 20 a	D26
D28	c 21 a	D27
GND	c 22 a	GND
D29	c 23 a	D30
D32	c 24 a	D31
GND	c 25 a	GND
Σg	c 26 a	GND
GND	c 27 a	GND
/CLK	c 28 a	CLK
/SEL	c 29 a	SEL
T_2	c 30 a	T_3
T_0	c 31 a	T_1
/LEAD-CLK	c 32 a	LEAD-CLK

Fig.5b

SHAPER CARD CENTRAL CONNECTOR
DIGITAL
POWER & DATA INPUT

c	pin	a
-5V	c 1 a	-5V
GND	c 2 a	GND
GND	c 3 a	GND
+5V	c 4 a	+5V
+5V	c 5 a	+5V
N.C.	c 6 a	N.C.
V_{bias}	c 7 a	N.C.
GND	c 8 a	GND
D31	c 9 a	D32
D30	c 10 a	D29
GND	c 11 a	GND
D27	c 12 a	D28
D26	c 13 a	D25
GND	c 14 a	GND
D23	c 15 a	D24
D22	c 16 a	D21
GND	c 17 a	GND
D19	c 18 a	D20
D18	c 19 a	D17
GND	c 20 a	GND
D15	c 21 a	D16
D14	c 22 a	D13
GND	c 23 a	GND
D11	c 24 a	D12
D10	c 25 a	D09
GND	c 26 a	GND
D07	c 27 a	D08
D06	c 28 a	D05
GND	c 29 a	GND
D03	c 30 a	D04
D02	c 31 a	D01
GND	c 32 a	GND

Fig.5c

4) Interrupted connection between the input analog connector and series resistors.
5) Shorted D1 or D2 diode.
6) Short to ground on the input analog line.
7) False soldering on the MC3430 chip.
8) Defective MC3430 in the input side.
9) Shorted C2 capacitor.
10) Open C2 capacitor or cold soldered.
11) Feedback resistor R_f altered or cold soldered.
12) Open C1 capacitor.
13) Shorted C1 capacitor.
14) Defective output of the MC3430.
15) Comparator chip without ground.
16) Comparator chip without positive supply.
17) Comparator chip without negative supply.
18) Short to ground at the output of the MC3430.
19) Interrupted line between the MC3430 and the SN74LS298 or false soldering.
20) Defective SN74LS298 at the input side.
21) Failure in the supply at the SN74LS298.
22) Defective SN74LS298 at the input side.
23) Defective V_{bias}.

Here is how to cure:

1) A false soldering on the central connector is equivalent to an open connection between the input line and the chip. The output, in this case, is seen as a zero. If there is a problem on the input connector, the test box stops twice, once in the analog test, the second time on the Σg test.
2) Same as above.
3) Same as above.
4) Same as above.
5) In this case the output is still seen as a "zero", but we have also a failure on the test lines.
6) If the short is downstream of the series resistor, we fall into the same case as above. Otherwise we have an output signal on the test lines.
7) The output is seen as a "zero".
8) The output remains low or high, insensitive with respect to input changes.
9) Either the output is high or the chip oscillates.
10) In this case one has no monostable effect. The output is high only when the input is more negative than the threshold.
11) If the resistor is cold soldered we have the same problem as above. If altered, we may have a shorter or wider output signal.
12) In this case the cross-talk level is lower, i.e. more cross-talk.
13) The same chip may oscillate and there can be multiple firing.
14) Same as 8.
15) The zero level output of the MC3430 rises to about 1 Volt.
16) The test box stops four times in the analog test, four times in Σg test, and also in the T_i tests.
17) Same as above.
18) The test box will always see a "zero".
19) The test box will always see a "one".
20) The test box will always see a "zero" or a "one".
21) In this case there will be troubles in the analog, in the digital and in the T_i tests, but no problem in the Σg test.
22) Similar to above. The box stops on the faulty line.
23) There is either multiple firing, if V_{bias} is shorted to ground, or incorrect output if V_{bias} is altered. The system also stops when testing Σg.

The Σg data path

If the test box has succesfully passed the analog test and it stops during the Σg test, there can be one of these failures:

1) Defective SN74LS126.
2) SN74LS126 without ground.
3) SN74LS126 without supply.
4) Broken interconnection between MC3430 and SN74LS126.
5) Broken interconnecting line between SN74LS126 and summing resistor.
6) False soldering on the summing resistor.
7) Broken interconnection between summing resistors.
8) False soldering of the Σg on the output connector.

Here is how to cure:

1) In this case the output transistor in the SN74LS126 may be permanently on. This is recognized by a LED on the front panel. When this LED blinks before pushing the START button, it is the indication that one of the transistors of the SN74LS126 in the "group of 8" is on; this can imply either a defective SN74LS126 or an interrupted connection between the MC3430 and the SN74LS126.
2) The zero level of the SN74LS126 is about 0.8 Volt.
3) In this case there are four transistors in the "group of 8" which do not switch on.
4) One "group of 8" is permanently on.
5) One " group of 8" is permanently off. The box stops 8 times.
6) Same as above.
7) Same as 5.
8) There is no output at all.

Test lines path.

If the board under test has succesfully passed the digital and the analog test, detection of a failure on the test lines can point to one of the following:

1) False soldering on the output connector.
2) Interrupted connection between the test lines and the base of the transistor.
3) Short to ground on the base of the transistor.
4) Defective transistor or false soldering.
5) Diode D_t open or cold soldered.
6) Interrupted connection between the emitter of the transistor and the cathode of D_t.

Clearly, if the test box has already halted on the analog data path, it also stops during the operations on the test lines, provided that the failure is downstream of the series resistors.

The above problems imply:

1) This failure can be intermittent. Once recognized, it is necessary to solder the points again; the test box sees this failure as an absence of test input signals; the outputs stay permanently at "zero", and therefore the test procedure halts 8 times.
2) Same as above.
3) Same as 1.
4) Same as 1.
5) In this case the test box halts only once.
6) In part similar to 5: more than one output fail.