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L. Rossi: A FAST CLUSTERING PROCESSOR FOR MULTIWIRE PROPORTIONAL CHAMBER READ OUT.

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ABSTRACT.

A processor is described which can perform clustering operation on 16-bit words. The use of ECL 10K circuitry allows processing times of $\simeq$ 100 nsec per word. On line transformation of data coming from a fast multiwire proportional chamber read out has been performed in an SPS experiment. A total of about 10^{10} clustering operations has been executed without appreciable error rates.

1. - INTRODUCTION.

A particle crossing a multiwire proportional chamber (MWPC) can induce signals on several contiguous wires thus reducing the spatial accuracy of the detector and increasing the number of words per event to be read out.

This effect, known as "clustering", has been extensively studied by several authors[1, 2, 3] and shows a clear dependence on the direction of the incident particle (Fig. 1) and on the width of the gate applied to the wire signals (Fig. 2).

The usual way of reducing the cluster size is to add an electronegative gas so that the sensitive zone is limited to a small region around the wire[4]. The effect of different percentages of such a gas is shown in Fig. 3. In a typical experimental situation, however, we cannot increase the Freon 13B1 percentage too much or decrease the gate width too much if we want to keep full efficiency for the MWPCs.

The compromise chosen, for instance in the WA7 experiment at CERN[5] - Freon 13B1 : 0.5%, gate width : 100 ns - gives rise to the cluster size distribution shown in Fig. 4.

From these data we can easily understand that the use of a hardware processor performing the clustering operation can considerably reduce the amount of words to be transferred to the computer.

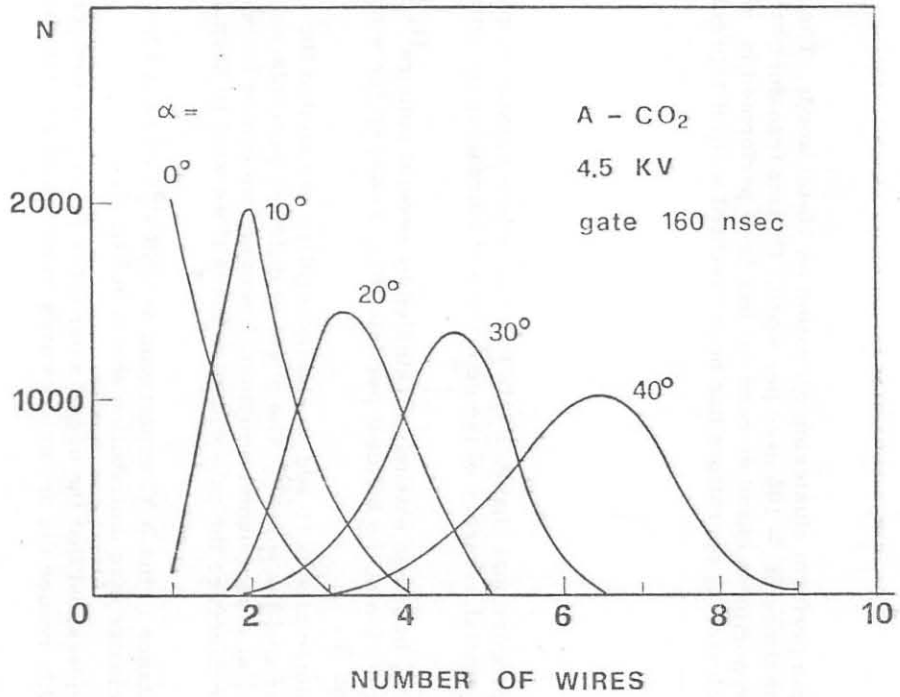

FIG. 1 - Wire cluster size as a function of the direction of the trajectories - Gate of 160 nsec (Ref. (2)).

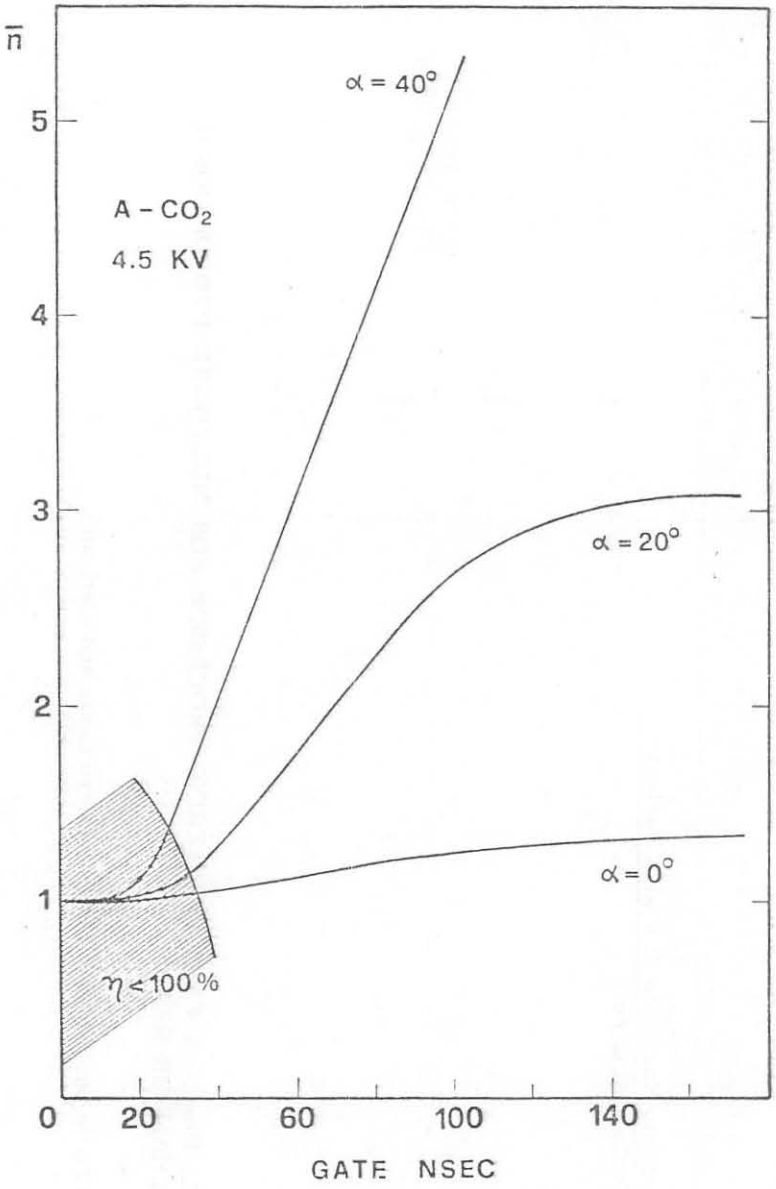

FIG. 2 - Wire cluster size as a function of time gate width. Wire spacing = 2 mm. Trajectories at 0°, 20° and 40° from the perpendicular to the chamber (Ref. (2)).

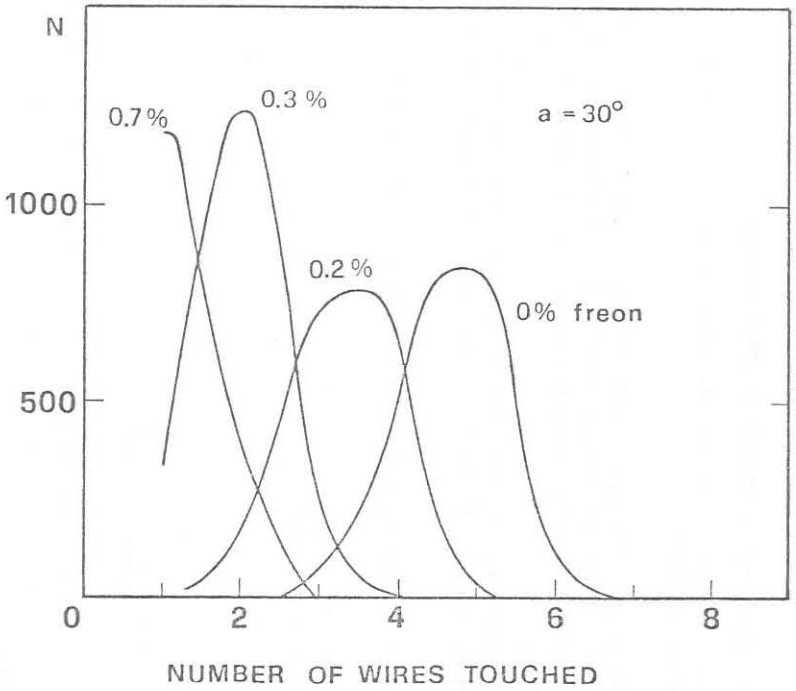

FIG. 3 - Wire cluster size with electronegative gases. Argon + Isobutane + Freon 13B1. Cluster size as a function of Freon 13B1 concentration (Ref. (2)).

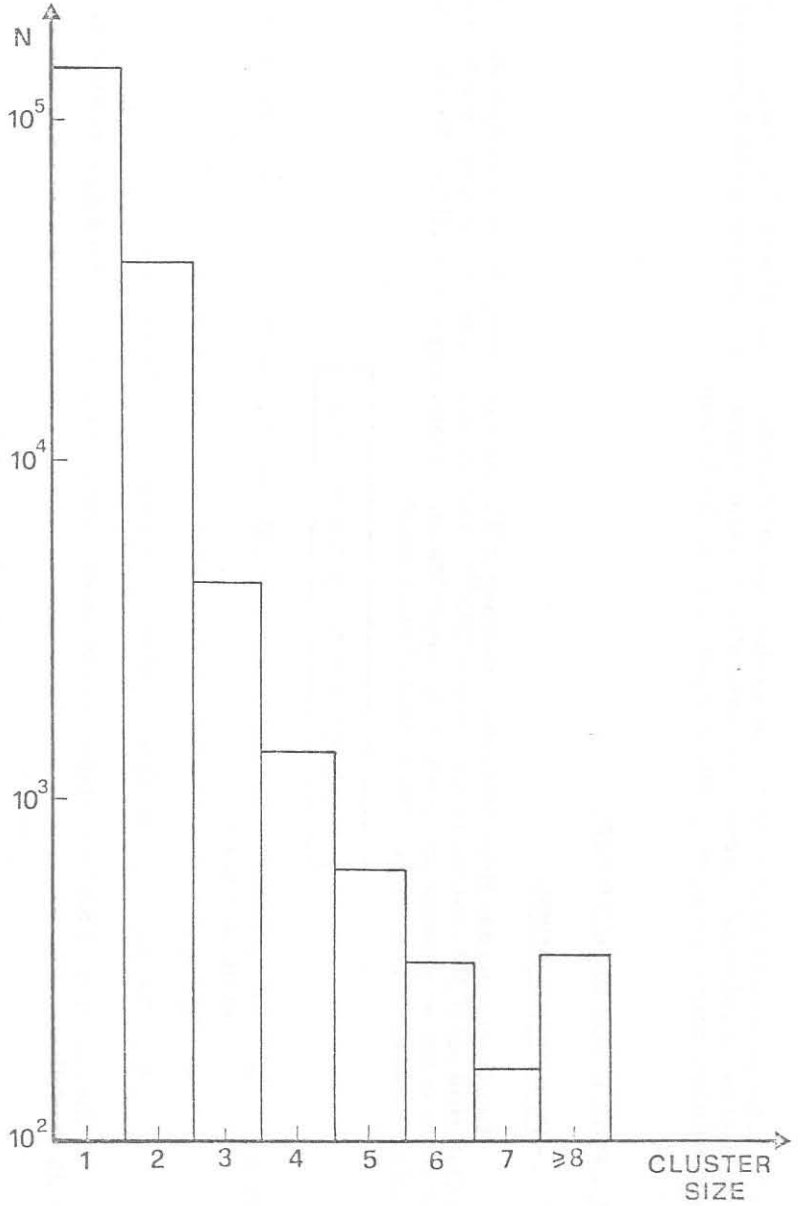

FIG. 4 - Cluster size distribution in the multiwire proportional chambers of the WA7 experiment. Chamber characteristics: wire spacing = 2 mm, gap = = 6 mm, gate width = 100 ns, Freon 13B1 percentage = 0.5 %.

If the processor is at least as fast as the read out system we can achieve this result without introduction of additional deadtime and pass already refined data to a more complicated processor (point finder, track finder, etc.) that will perform on-line filtering.

2. - PROCESSOR DESCRIPTION.

2.1. - Input/Output format.

The Clustering and Renormalizing processor (CRN) has been designed to be compatible with a fast read out (RMH system) developed at CERN[6]. This system gives the hit addresses as a set of 16 bit words at a maximum speed of one word/120 nsec obtained by use of MECL 10K circuitry and handshake-mode dialogue. The format of these words is :

F X N N N N N N N N N N N N N N

where : N = Hit address, increasing from 0 to 11263 ; in the case of F = 1 N is the start address of the new plane.

X = Not used.

F = Flag bit. Only the first word of a new plane contains this bit.

The aim of the CRN is to compress consecutive channel addresses into single data words with the following format :

F C C C C C C C C C C C C C S S S

where : S = Cluster(x) size { S = ∅ means single wire cluster; S = 7 means cluster of ≥ 7 wires.

C = Cluster centre, in half wire units ; up to 4095 (i. e. 2047 wires).

F = Flag bit. It has the same meaning as in the normal read out but is now associated with the first wire address in the plane.

This data transformation reduces the length of a typical proportional chamber block by 30% in the WA7 experiment, but it is possible only if data have been previously renormalized (i. e. each new plane will start at address zero) because that multiwire proportional chamber system, like most of the existing ones, exceeds 2000 wires.

The sharing of information between cluster size and centre has been decided taking into account the large size of the WA7 proportional chambers[7] and the expected cluster size distribution[1, 2, 3] for this apparatus.

A second output format is, however, foreseen for those experimental situations where very big clusters can be encountered :

F C C C C C C C C C C C C S S S S

Moreover the special word

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

(x) A cluster is defined as a set of adjacent hit wires. In the particular case of a "single-wire--hole" inside a physical cluster we can have either two separate clusters or a single one, depending on constants set by hardware.

is generated if an empty (i. e. without hit wires) plane is detected. This is, in particular, useful for fast rejection of data through a hardware processor.

Rough information on wire chamber events can be directly extracted from the CRN. Two NIM[8] signals are available ; the first one is given if the number of empty planes in the whole read out chain is bigger than a selected value, the second one if the number of clusters in a plane exceeds a chosen number.

If a fast decision is taken by the external logic (NIM circuits, processors, etc.) and we are not anymore interested in further MWPC data we can send a NIM signal to the CRN to terminate the read out and reset the chamber data.

2. 2. - Data transmission.

The exchange of information between the read out system and the CRN as well as between the CRN and the external circuits is done via a double handshake method ; its principle, shown in Fig. 5, is very simple : we have an "asking" and an "answering" circuit, the first one starts the conversation sending a START READ and soon after, a request for data (ENCODE) ; the second one reacts by giving these data - as soon as they are ready - together with a DEVICE FLAG strobe. The ENCODE-DEVICE FLAG cycle is repeated up to the end of the available data, then the last ENCODE produces a DEVICE FLAG and an END OF RECORD (EOR).

After EOR a RESET signal can be sent out by the "asking" circuit, if we do not want to reread the same information from the read out system.

The timing diagram of these signals is shown in Fig. 6. A computer controlled by-pass capability - that is mainly useful for test purposes - can be added to the CRN processor.

2. 3. - Logic.

The logic of the CRN is schematized in Fig. 7. The architecture of this processor is designed to obtain the maximum speed possible with current technology. The use of three independent Arithmetic Logic Units (ALU), of precision delay lines for clock propagation, and the absence of memory - except the registers for temporary word storage - are the main means to reach this aim.

The CRN behaves as follows :

a 16-bit word is memorized in Register 1 each time a strobe is received from the read-out ; the same word is recorded in Register 2 if bit 15 is set.

Then, after a delay corresponding to the maximum propagation time of ALU 1, the result of the subtraction R1-R2 will be kept in R3 if the incoming word has been recognized as a wire address (i. e. if it is carrying physical information). In R3 we have renormalized data ; from here onwards the calculations to obtain the final word are executed on 12 bit words only.

The renormalized address is moved to R4 after a 40 ns delay if it is not the first wire address found in the current plane. In fact the following operation - i. e. the comparison between two successive words to see if their addresses differ by 1 or more (ALU 2) - would not be meaningful in that case.

Depending on the result of ALU 2, we can do two things :

a) The difference is 1. Then we build up a cluster clocking the cluster size counters[x].

b) The difference is greater than 1. Then the cluster is finished and the result have to be saved. Hence the data is stored in the register R5 in which :
   i) the 3 least significant bits are simply the cluster size counter (C1) content;
   ii) the 12 following bits are the result of the operation 2R4-C2 and since R4 still holds the last word of the cluster, this is the cluster centre in half wire units;
   iii) the most significant bit is the flag bit.

(x) Two different counters are used for cluster size measurement. C1 is a 3-bit counter that goes up to 7 and than halts ; C2 is a 12-bit counter for precision measurement of cluster centre in case of large clusters.

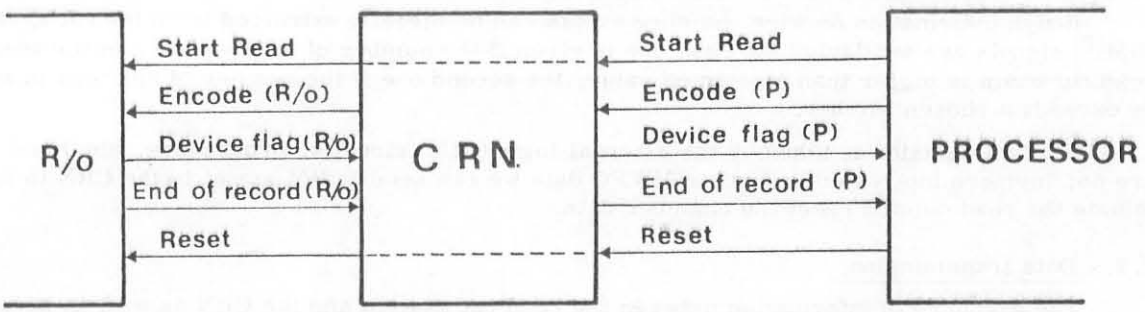

FIG. 5 - Scheme of the dialogue between CRN and external circuits.

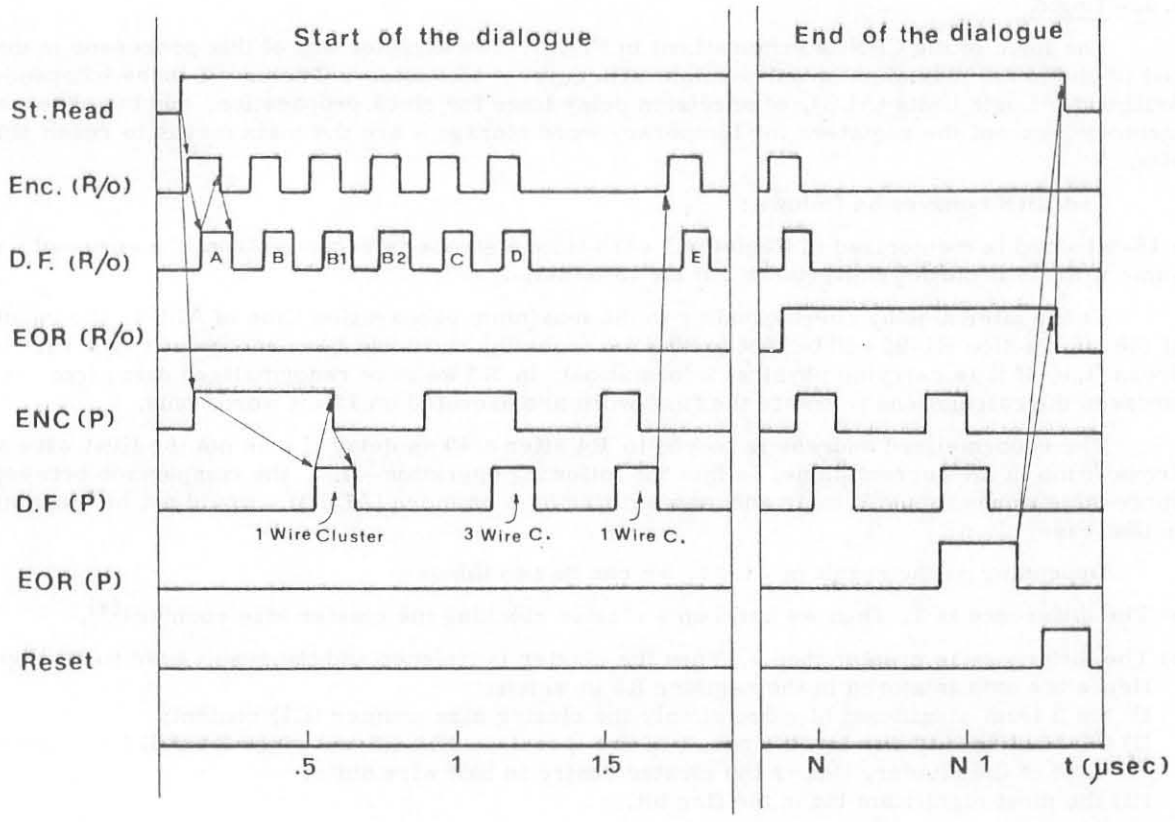

FIG. 6 - Timing diagram of dialogue signals.

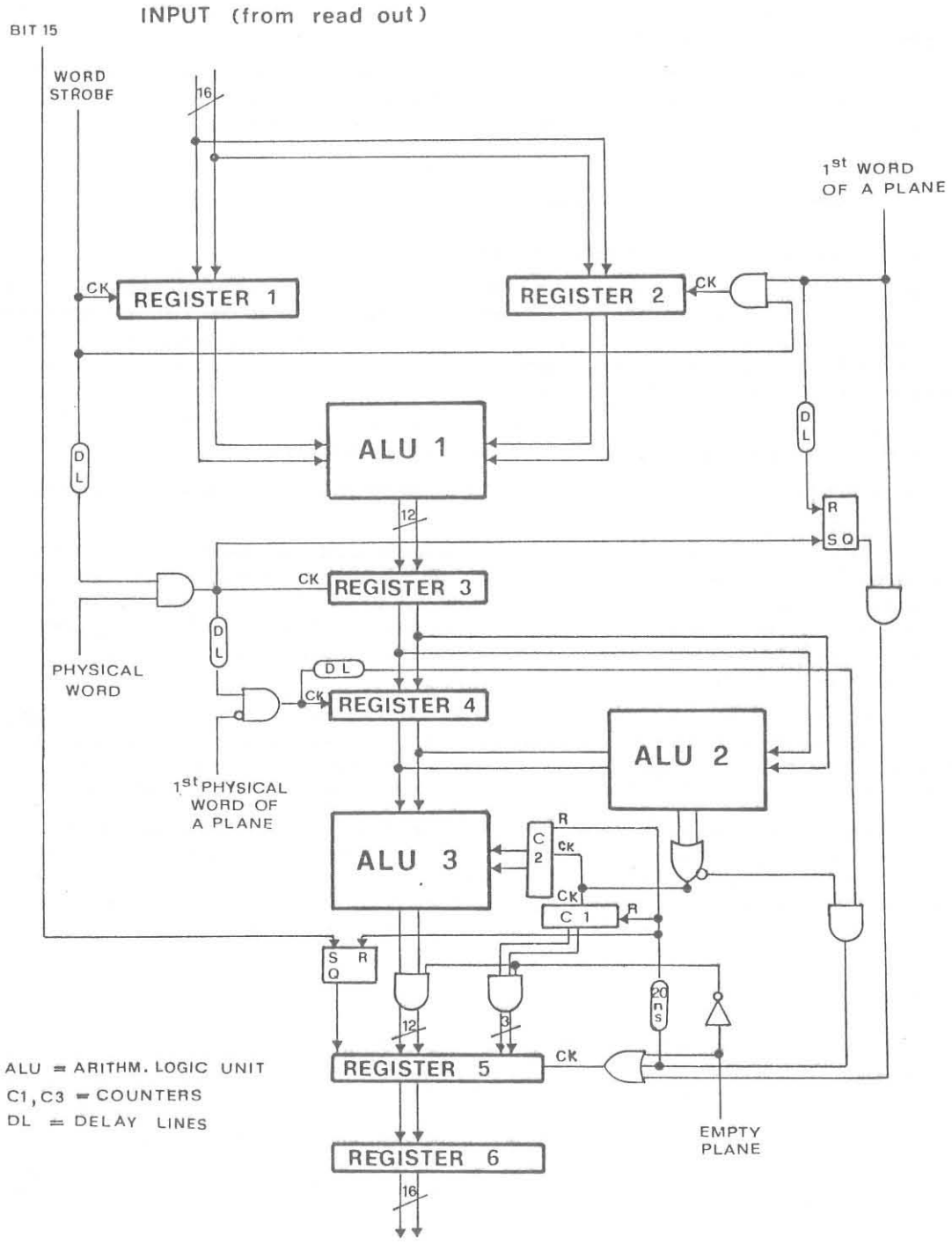

FIG. 7 - CRN logic scheme.

We also decide that a cluster is finished when a plane is finished. Moreover we write in R5 bit 15 set followed by all zeros when we do not detect wire information between two consecutive words with bit 15 set (EMPTY PLANE).

The use of two consecutive output registers - 5 and 6 - permits building up a new cluster even with a word ready for reading. A busy logic (not shown in Fig. 7) will block the transfer of data from the read-out to the CRN if both output registers are filled.

3. - PROCESSOR TEST AND OPERATION.

The processor has been set up in two steps.

The first test of the circuit was done in the following way : simulated data were injected into the memory of the read out via word generators ; they were read out with and without the CRN; a software transformation (the same that the CRN does by hardware) is applied to the second data and a comparison with the first ones is performed, after 10^5 cycles without errors the CRN is considered to be working with that set of simulated data.

If this is not the case a faster program, that simply reads the CRN, is used and investigations on the internal status of the processor are done with a logic analyzer.

Since not all possible configurations of bits can be checked via this method an additional procedure is required.

The CRN is then used in an experiment with a proportional chamber system consisting of 2×10^4 wires[5] and its behaviour is monitored with on-line programs. Off-line analysis on 10^8 clustered events shows the same track reconstruction probability as it does on the same amount of unclustered events previously recorded with the same apparatus. This proves that the CRN is behaving properly and steadily over a long period of data acquisition (few months) which is needed in high energy physics experiments.

The use of the CRN becomes more attractive if we want to correlate data coming from proportional chambers using a hardware processor ; in this case the compactness of clustered data will reduce considerably computing time and allow for faster answers to the correlation requirements ; moreover as the CRN (Fig. 6) does not introduce any additional deadtime.

A complex hardware processor[9] has been used in the WA7 experiment for coplanarity and opening angle checks on elastic candidates. The timing diagram of its dialogue with the CRN is shown in Fig. 6. A maximum speed of 3 words/μsec (to be compared with the 0.5 words/μsec of a CAMAC[10] cycle) is obtained with a 10 meters long cable between the CRN and the processor.

4. - CATHODE READ OUT.

It is known that the signal induced on the cathodes of a proportional chamber is spread out on a zone of several square millimeters[11]. If the cathodes are built up of wires spaced 1 mm and the pulse height on each channel is recorded, the avalanche centre can be determined by off-line methods with a precision of 150 μm, weighting the contribution of each wire[12]. Since the avalanche is symmetric around the track coordinate the use of a CRN in connection with a cathode read out will allow, in that case, the measurement of a particle intercept with ~ 500 μm precision (half wire spacing). On-line operation and data compression will balance this loss of accuracy.

Two coordinates can be extracted by this method from a single proportional chamber thus avoiding "ghost points" that can arise from independent chambers with perpendicular anode wires.

5. - CONCLUSIONS.

A hardware processor performing clustering operations (CRN) has been built in Genoa and tested in an experiment at CERN. Its high speed makes it especially suitable for use with mo

re complex processors. The CRN had shown to be useful in connection with anode read out of a proportional chamber by minimizing the number of words to be transferred to a computer. Lastly it can make point finding operations easy when applied to cathode read out.

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