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THE SILICON LABORATORY IN UDINE: QUALITY ASSURANCE TESTS ON THE WAFER SENSORS FOR THE ATLAS PIXEL DETECTOR

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Abstract

In this note we describe the set-up that has been implemented in the Silicon laboratory at the Physics Department of the University of Udine, in order to perform the quality tests on the wafer sensors for the ATLAS Pixel Detector. The Quality Control Procedure to be fulfilled by the participating institutes is described in an ATLAS protocol. At our institute the pre-production measurement phase has recently been completed, while the production phase is running. A brief description of the measurements and a summary of the results obtained are also presented.

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1 INTRODUCTION

For the ATLAS detector at LHC (CERN), which is scheduled to start taking data in 2007, it is requested a high rate suitability and radiation tolerance for rates of proton-proton collisions of 40 MHz at $\sqrt{s} = 14\text{TeV}$. In particular, the innermost layers have to detect high particle track occupancies per layer unambiguously, and for this reason it was decided to use small pitch pixel detectors.

The ATLAS Pixel detector[1)] at the LHC, which is currently under construction, provides critical tracking information for pattern recognition near the collision point, and largely determines the ability of the Inner Detector to find secondary vertices. The Pixel Detector will consist of three barrel layers and three disks in each forward direction. The smallest detector unit will be a module made of one silicon pixel sensor and sixteen read-out chips connected with high-density bump bonding techniques to the sensors.

A Pixel sensor is a 16.4 x 60.8 mm wafer of silicon with 46080 pixels, 50 x 400 microns each. A Pixel module comprises an un-packaged flip-chip assembly of 16 front-end chips bump bonded to a sensor substrate. There are 1744 modules in the Pixel Detector for nearly 80 million channels in a cylinder 1.4 m long and 0.5 m in diameter, centred on the interaction point. The barrel part of the pixel detector consists of the three cylindrical layers at a radial position of 50.5 mm, 88.5 mm and 122.5 mm respectively. These three barrel layers are made of identical staves inclined with an azimuthal angle of 20 degrees. There are 22, 38 and 53 staves in each of these layers respectively. Each stave is composed of 13 pixel modules. In the module there are 16 front-end (FE) chips and one Module Control Chip (MCC). One FE chip contains 160 rows and 18 columns of pixel cells, i.e. 2889 pixels per FE chip or 46080 pixels per module.

There are three disks on each side of the forward regions. One disk is made of eight sectors, with six modules in each sector. Disk modules are identical to the barrel modules, except for the connecting cables. The front-end chips are a major heat source (0.8 W/cm^2) dissipating more than 15 kW into the detector volume. This heat is taken out via integrated cooling channels in the detector support elements: Staves in the barrel region and Sectors in the forward region.

2 THE SENSORS FOR THE PIXEL DETECTOR AND THE QUALITY ASSURANCE STRATEGY

The ATLAS pixel sensors will have to withstand high radiation level (a particle fluence up to 10^{15} cm^{-2} and an ionisation dose up to 500 kGy of mainly charged hadron radiation) to stay fully operational for the scheduled 10 years operation at the LHC. The technology chosen for these sensors consists of n^+ implants on a high resistivity n-bulk substrate, using a moderate p-spray technology for inter-pixel isolation between the n+ implants of the sensor pixel cells[2), 3), 4)]. It has been demonstrated that p-spray is radiation hard [5)], and allows punch through biasing via a bias grid also for sensor testing before assembly. In 2001, ATLAS has chosen two firms for the production of all the sensors (2000) needed for the Pixel detector: *CIS* and *Tesla* (from the end of 2003 its name has changed to *ON Semiconductor*)[6)], both

having to produce 1000 sensors. The group of Udine will perform the quality test on one fourth of the total production (500 sensors). The rest of the sensors will be tested in Dortmund, New Mexico and Prague.

To ensure a correct functioning of the pixel detector layer and to find and minimize possible problems in the manufacturing process, dedicated testing routines have been implemented. For the pixel sensors, whose production started in 2001 after an intense prototyping phase[4] the Quality Control Procedure Protocol and routines have been implemented with the start of pre-production.

Testing procedures and test results are continuously monitored and cross-checked between the sensors manufacturers and the four testing institutes. The sensors arrive to the testing sites structured in a wafer. A wafer contains three sensors *tiles* of the size to be used for the ATLAS modules (16.4 x 60.8 mm^2) and several additional test structures (see Figure 1). Each tile contains 328 x 144 pixel cells of size 50 μm x 400 μm, 250 μm thickness. These will be connected to 16 front-end chips by using bump bonding and flip chip technology.

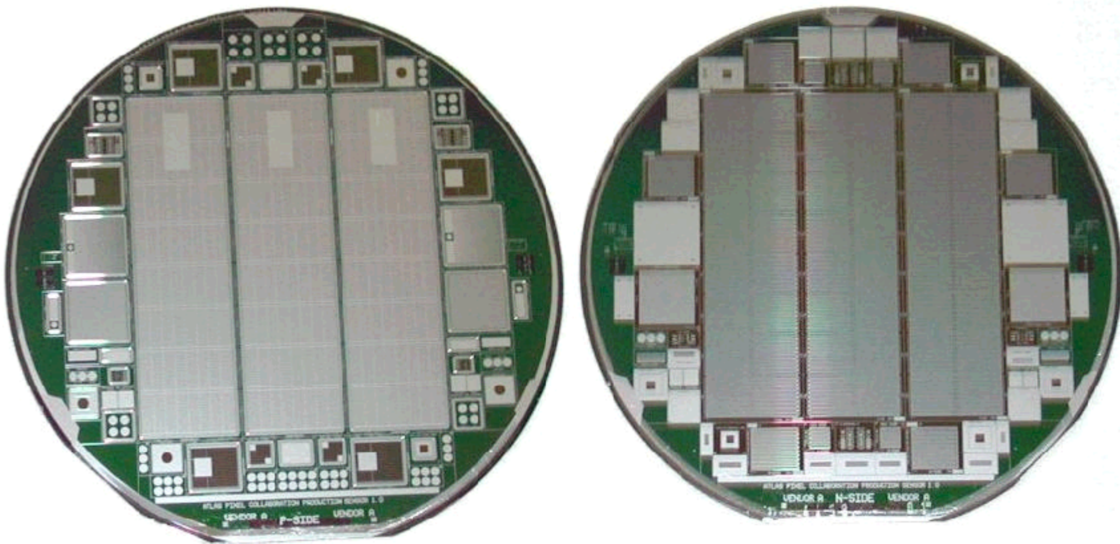


FIG. 1: p and n side view of a sensor wafer.

The main aim of testing is to collect data useful for sensor operation as early as possible, while preventing damage to the sensors. Exactly for this reason, on the wafers, together with the three sensors, there are other dedicated test devices (in Figure 1, for example, the three tiles, the nine single-chips and the four mini-chips are clearly visible), custom designed for specific diagnostic tests. They allow for relatively easy measurements on the production wafers, avoiding a strong impact on the tile sensors by repeated probing.

Apart from one basic functionality test to be performed on each sensor, the diagnostic tests are performed either on each wafer or only on a small sample from each production batch.

The test procedures belong to two basic categories:

1) Tests performed directly on the three full size sensor tiles later to be used for detector assembly.

In order to reduce the sensor tiles manipulation and risk of damages, only a voltage tolerance test (I-V characteristics up to 500 V) is being performed on each tile. Measurements of time stability are taken on one tile per production batch only.

2) Diagnostic tests on test structures present on each sensor wafer

These measurements cover a wide range of characteristics important for detector operation and monitoring, of sensor production, including wafer thickness, substrate resistivity, bulk capacitance, depletion voltage, oxide quality and capacitances, inter-pixel isolation and capacitance, p-spray dose, punch-through voltage. Each structure is sampled a few times to provide more chances to get a good result, in case some structures fail to pass the test.

Both CIS and Tesla produced and delivered 14 pre-production wafer sensors (that is 52 sensors). In 2002 the real production is started and up to now (December 2003) Udine has received all the 250 sensors (about 100 wafers) from CIS while the first production wafers from Tesla should arrive in January.

3 THE SILICON LABORATORY IN UDINE

The history of the Silicon laboratory in Udine, starts in 1995, when the proposal of Profs. C. Del Papa and F. Waldner to help in the design and test of the sensors for the Pixel Detector in ATLAS, is approved in an INFN meeting of Gruppo I in Genova. With the encouragement of Prof. L. Maiani, the President of INFN, in 1996 the INFN grants the funding for the instrumentation, probe station and software for the sensor design phase.

In the same period, the Rector of the University of Udine, Prof. M. Strassoldo, supports the construction of the clean room, and finally the library of the Physics Department is moved to make space to the new laboratory. At the end of 1996, the instrumentation for the IV ad CV measurement (see Chapter 4) is working, a deposit for the radioactive sources exists and the test structures for the sensors are designed. In February 1997, the clean room is built, a concrete block to support the probe station is ordered from a local firm.

In March the probe station is installed and in November the fist wafers (from Seiko) arrive at Udine to be measured. A probe card is ordered as well. In 1998 a climatizer, a freezer, a wire-bonder machine and an oscilloscope are bought.

The laboratory has been entitled to the memory of Maurizio Innocente, a former student of Prof. F. Waldner.

Nowadays the laboratory consists of an outer part for testing the assembled detectors and a clean room for handling sensor wafers and electronic chips. The clean room is approximately 18 m^2 (figure 2 shows an outside view of it).

The floor is made of a special conducting plastic material, to reduce the possibility of electrostatic discharges. Conducting heels will be worn over the overshoes to connect the operators to ground and avoid wire connections with bracelets. The room is air conditioned, to guarantee operation temperatures in accordance with quality protocol requests. Inside the clean room a semiautomatic probe-station (figure 3) is placed in a stainless-steel dark box.

The instrumentation for measuring the detector parameters is also shown in figure 4. It presently includes:

one Keithley 237 (1000 V voltage source - picoammeter);
one HP 4284A LCR meter 20 Hz - 1 MHz;
one Maehlum1-side probing station, with three arms and two H.V. arms;
one 2-side probing station (kind present by the University of Dortmund)
one Micos X-Y+Z stage and controller;
one Keithley 6514 electrometer;
one Keithley 487 picoammeter – voltage source;
one Keithley 486 picoammeter;
one HP E3631A triple output power supply;
one HP 3620A dual output power supply;
one Olympus SZ60 microscope, stereo, 100X;
one Leica MZ8 microscope, stereo, 50X;
one Optiphot 150 microscope, 1000X;
one CCD color video camera;
one Eichhorn and Hausmann MX301 thickness gauge.

They are PC controlled via GPIB and Labview software. The probe station is placed

on a concrete bench made out of a single block, weighing approximately 500 kg, to improve stability (figure 4). The feet are directly placed on the table so that the probe station is mechanically decoupled from the shielding cabinet. The probe station and the control software have been made by Maehlum Instruments s.n.c.. The chuck is motorised, with X-Y-Z computer controlled movements. A map of the bonding pads to probe can be loaded in the Labview software for automatic testing of a whole wafer. The microscope Olympus SZ60 is equipped with a CCD camera connected to a PC. The probe manipulators are made by Karl Suss (PS100).

The whole set-up has a leakage current of 500 fA, with a triax cable connection up to the shielding box and a coax cable to the probe head. Preliminary tests have been made on silicon strip detectors, then measurements on the ATLAS Pixel Prototype wafers have been performed.

For testing double sided Silicon detectors a special pressurized "chuck" (figure 5) is needed. Pneumatic tubing, pressurised one at the time, are connected via a pass-through system to a 6-bar gas line (figure 6).

FIG. 2: The clean room as seen from outside.

FIG. 3: The probe station and the dark box on the single block table.

FIG. 4: The rack with the electronic instrumentation near the dark box.

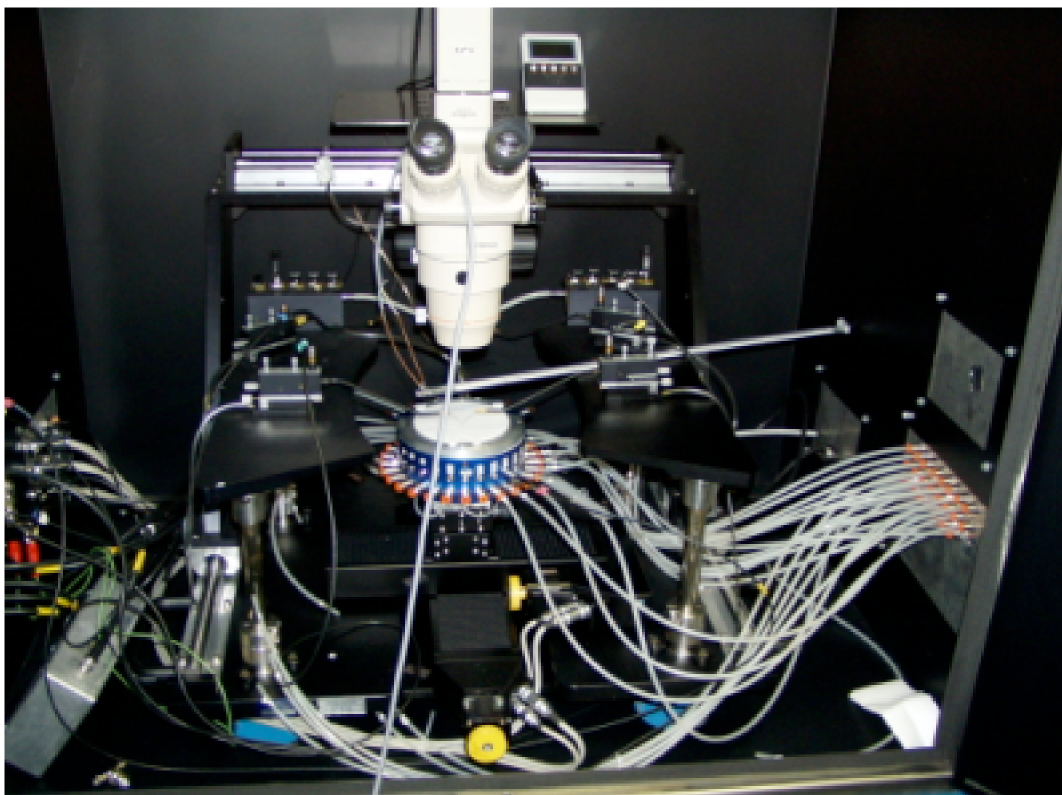


FIG. 5: The probe station with the pressurized chuck.

FIG. 6: The gas lines.

4 THE MEASUREMENTS

The quality tests on the wafer sensors are done at our laboratory according to the ATLAS Pixel Sensor Quality plan[7]. They consist of optical, mechanical and electrical test measurements on pixel sensor wafers performed in a clean room with separated, filtered air ventilation and environmental control to guarantee standard conditions in temperature (between 20ºC and 24ºC) and relative humidity (less than 50%). To assure comparable results over the whole period of quality measurements and between the different labs participating to the measurement process, calibration and cross calibration are also of primary importance.

The measurements presented here have been performed on the pre-production wafers (for a total of 28, 14 from CiS and 14 from Tesla), and on part of CiS production wafers delivered to Udine. Since the beginning of the production phase, which started in July 2002, 96 wafers from CiS have been tested (almost completely) at our laboratory, corresponding to 87% of our share of the vendor's production. The time estimated to fully test one wafer is of about one day. A total of 4 wafers were broken during manipulation by the operators. Until now the number of wafers that have been rejected for not being compliant with quality specifications is also 4.

The pre-production phase was a feedback process, which is the result from the ATLAS laboratories were used by the vendors to correct production problems. This will be apparent in a comparison of the plots for the pre-production and production measurements.

As a general rule, there are wafer-based and batch-based measurements, meaning that either all wafers or only some wafers per batch (usually one or two) are to be measured. In case a batch-based test fails, all wafers in the batch have to be checked for the same test, to sort out the bad ones. All the data collected are then saved in the PIXEL production database (PDB). The PDB is based on the ORACLE database management system. The main ORACLE server is set in the Geneva University on a dedicated Sun Enterprise station and the access to the DB is limited to the authorized people in order to keep secure the information. This system will make possible to always access the main data and will allow the tracking and monitoring of the most interesting parameters.

4.1 Optical and mechanical tests

4.1.1 Visual Inspection

Each wafer is inspected by checking mask alignment structures, identification pattern correctness and visible irregularities or mechanical damages. The equipment consists of a microscope (at least 1:60 magnification), and a microscope-mounted camera, with the possibility to store pictures as computer image files. The visible alignment tolerance between mask pairs is 2μm.

During the visual inspection phase several different irregularity categories were identified; no clear correlation with poor electrical behavior was detected, so finally only visible damages such as scratches on the wafers have been flagged. Figure 7 a) shows an image example of a detected scratch, while figure 7 b) shows one of the four mask alignment monitors on a wafer.

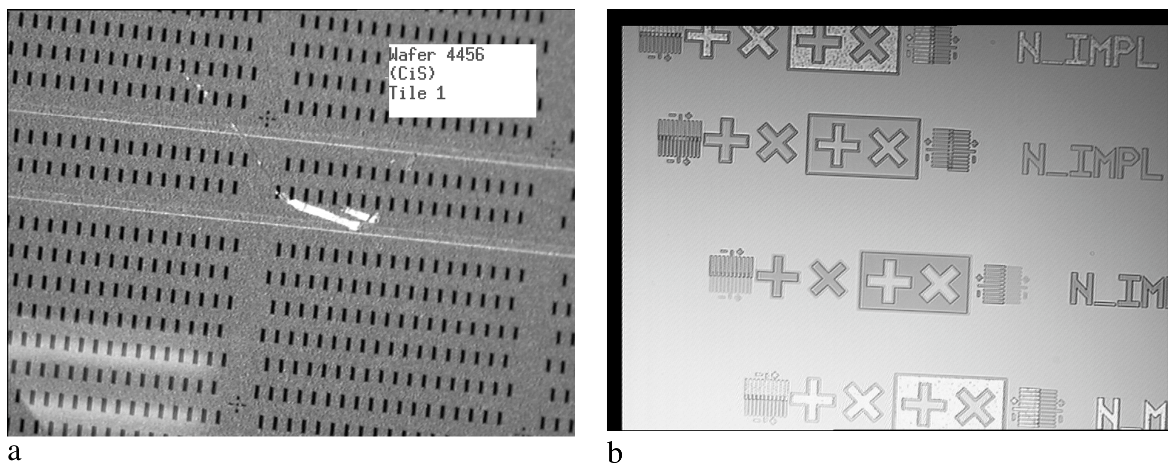


FIG. 7: a) Detected scratch on a tile, b) Mask alignment monitor.

Figure 8 shows a defect affecting several pixels, covering a large part of the three tiles on production wafer CiS 5430-04. This wafer has been rejected.

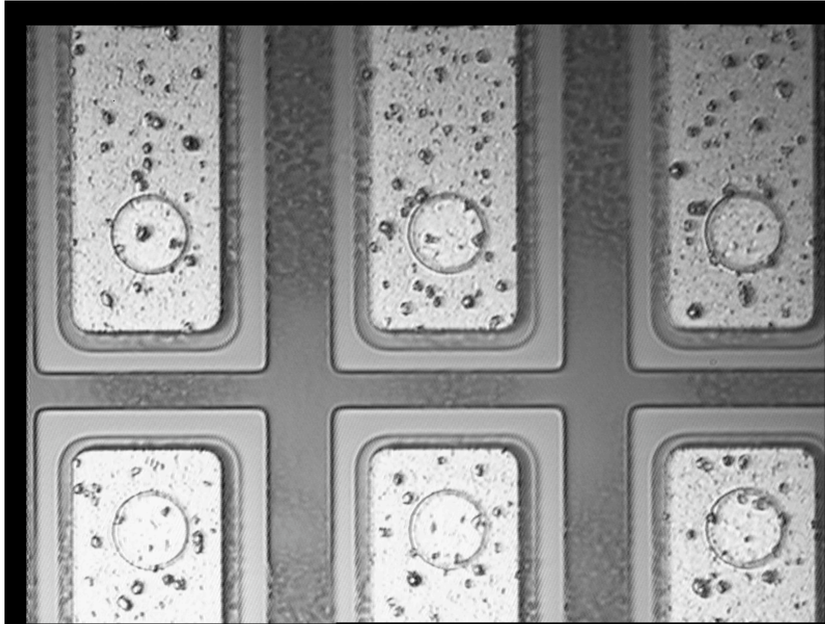


FIG. 8: Detected defects affecting pixels.

A summary of the relevant quantities resulting from the visual inspection is shown in Table 1. From the first line we see that the ID scratch patterns have been nearly always correctly done by the vendors.

TAB. 1: Visual inspection controls on pre-production and production sensor wafers

	Pre-production		Production
	CiS	Tesla	CiS
Scratch pattern correctness (good / total wafers)	12 / 14	13 / 14	86 / 86
Mask alignment. < 2 μm (good / total wafers)	8 / 14	7 / 14	9 / 62

The very low yield on CiS production wafers deserves few words. Our measurements showed a systematic problem on one mask pair. Fortunately the non-compliance resulted to be acceptable, since our limit was unnecessarily strict. Only one wafer was out of specs by more than 2.5 μm, and was rejected. Moreover, feedback from our lab allowed the vendor to correct the problem starting from July 2003 deliveries.

Also Tesla experienced problems with mask monitor fabrication; our measurements were fed-back to them as well.

Since the pixel design is pulled to the present technical limits, this measurement is especially important for estimating alignments of pixel implantations and possible effects on their functionality. Most of the wafers, especially pre-production ones, showed mechanical

scratches on some structures, an inevitable consequence of manipulation and measurement. In particular some tiles presented scratches on a f

ew (or a few tens) pixels. None of these were judged so severe as to reject the tiles.

4.1.2 Planarity Measurements

All pre-production wafers and one randomly chosen wafer from each production batch are measured for planarity. A wafer is placed on the X-Y-Z stage and the z coordinate (that is the coordinate orthogonal to the wafer surface) is measured over a matrix of points covering the tile area on the wafer. This restriction is due to the method used for the measurement, since only areas like the ones containing the pixels have the necessary optical contrast. The z coordinate surface is determined by measuring the stage position giving the best focusing from a set of images acquired with a CCD camera mounted in place of one of the oculars of a stereo microscope. The focal plane position is determined using a maximization algorithm[3)], giving $\sigma_Z < 4$ μm.

The resulting profile over a matrix of 169 points is then corrected for the tilt of the optical axis of the microscope. The image collection and the translator movements are managed by two server processes running in a Labwindows environment. A third process, running in a CVI environment handles the TCP/IP communications to the other processes and performs the DIP (Digital Image Processing) and filtering needed for the task The acquisition and analysis are completely automated; the time needed is < 50 s per scan point (PII 330MHz). The wafer planarity is defined as the distance between two planes, parallel to the average plane, enveloping the entire matrix points, and is required to be < 40 μm.

Figure 9 shows an example of software reconstruction of the wafer surface, units on all axes are microns. Results on the planarity measurements are shown in Table 2.

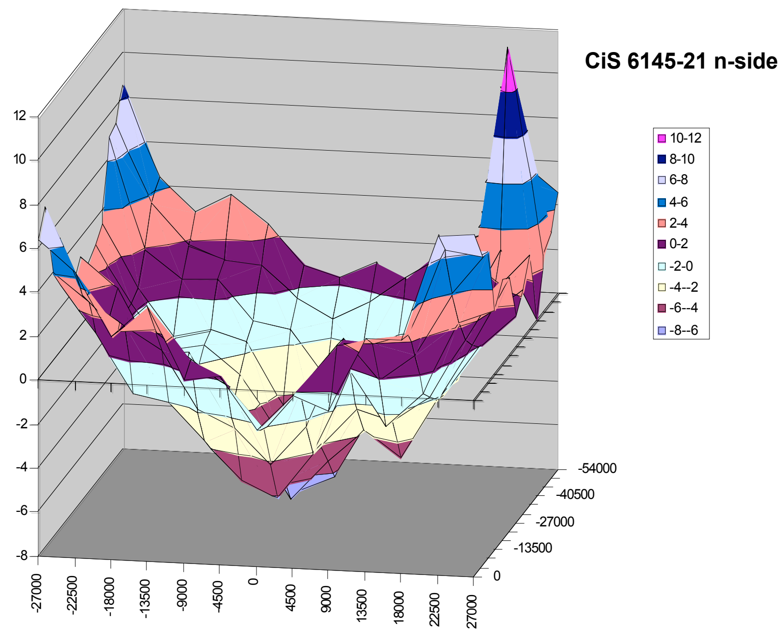


FIG. 9: Software reconstruction of wafer surface (units on all axes are microns).

TAB. 2: Planarity controls on pre-production and production sensor wafers. In parentheses the total number of measured wafers is specified.

	Preproduction		Production
	CiS (14)	Tesla (13)	CiS (28)
Planarity < 40 μm (% good)	100	88.9	100

4.1.3 Thickness Measurements

After wafer cutting, two opposite test sector pieces of one randomly chosen wafer from each batch are measured using a micrometer. The thickness is measured near the two planarity marks. The two measured thickness values are required to be between 220 and 260 μm, and the approximate thickness uniformity, defined as the difference between the two values, must be < 10μm. These measurements are supposed to be done with a mechanical micrometer on cut wafers. However this would mean waiting for months after the electrical measurements have been done, to have the pieces back from cutting, while the thickness information is needed from the beginning. Therefore we decided to use a capacitive, contactless gauge to do the measurement (the use of a contact gauge on integer wafers is excluded for safety reasons). 28 wafers from CiS production have been measured and all complied with QA requests. Figure 10 summarizes the measurements.

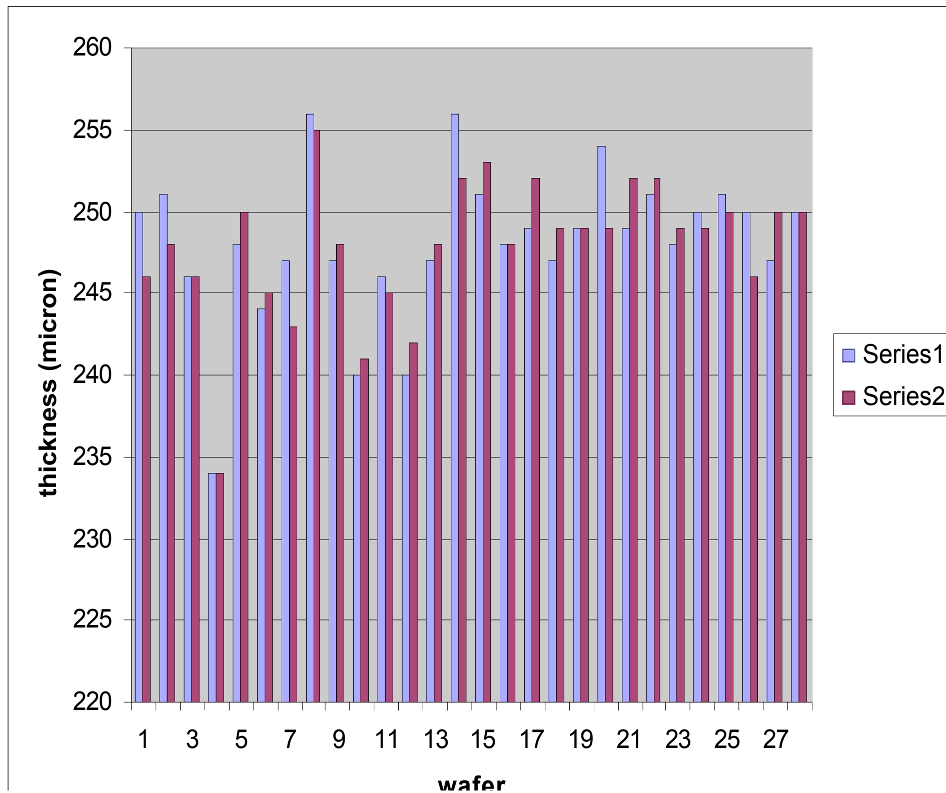


FIG. 10: Thickness measurement on 28 wafers. The two series refer to the two measurement sectors on the wafer.

4.2 Electrical tests

In all current-voltage measurements a breakdown voltage is defined, which is somewhat different from the usual definition for a semiconductor diode. In the contest of our measurement we define as breakdown voltage, the maximum voltage that gives a current less than a predetermined value.

Since leakage current is sensitive to temperature and it is unpractical to make all measurements at exactly the same temperature, a compromise has been taken: during measurements, temperature must lay between 20 and 24 °C and a formula is used to reduce (normalize) the data to the reference temperature of 20 °C.

4.2.1 Current-Voltage and Capacitance-Voltage measurement on diode with guard rings.

On each wafer the I vs. V characteristic of one diode with guard ring has to be measured to determine its breakdown voltage as preliminary to the capacitance-voltage measurement. The equipment consists of a probe station with chuck and needles for two contact points, a voltage source and a picoammeter.

The low (ground) voltage side of an LCR-meter is connected to the diode contact pad on the p-side. The metallised n-side ring of the diode is connected to the high voltage side.

The high voltage is stepped through, from 0 V to $-V_{bd}$ (the breakdown voltage) or –500V (later changed to -200V), whichever is higher in absolute value.

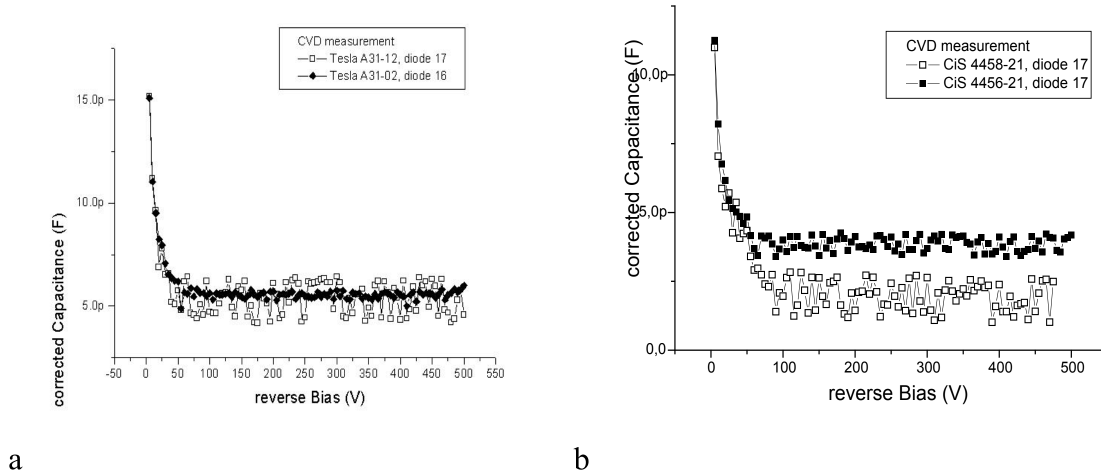
The relevant parameters are the depletion voltage V_{dep} and capacitance C_{dep}, the operation voltage V_{op} and the resistivity ρ. V_{dep} is the voltage at the sharp bend levelling into a plateau in the C-V plot (usually between 50V and 120V). C_{dep} is the capacitance at V_{dep}. V_{op} is defined as the maximum between 150 V and (V_{dep} + 50 V). The resistivity is computed as:

$$\rho = d^2/(2 \cdot V_{dep} \cdot \mu_e \cdot \varepsilon_{Si} \cdot \varepsilon_0)$$

where d is the sensor thickness (in microns), $\mu_e = 1427 cm^2/Vs$ the electron mobility, ε_{Si} = 11.75 the dielectric constant for Silicon, $\varepsilon_0 = 8.854 \cdot 10^{-6} pF/\mu m$ the permittivity constant.

The quality assurance (QA) requirements are: 30 V ≤ V_{dep} ≤ 120 V and 2000 Ωcm ≤ ρ ≤ 5000 Ωcm. The resistivity requirement is a standard for detector-grade silicon.

Figures 11 a) and b) show the Capacitance vs. Voltage curves for different diodes from Tesla and CiS pre-production, respectively. A high noise is visible in the plots; to remove it to some extent, we decided to average a set of measurements taken at the same voltage. In figure 12 Capacitance vs. Voltage plots for production wafers are shown.



a b

FIG. 11: Capacitance vs Voltage measurements for a) Tesla and b) CiS diodes.

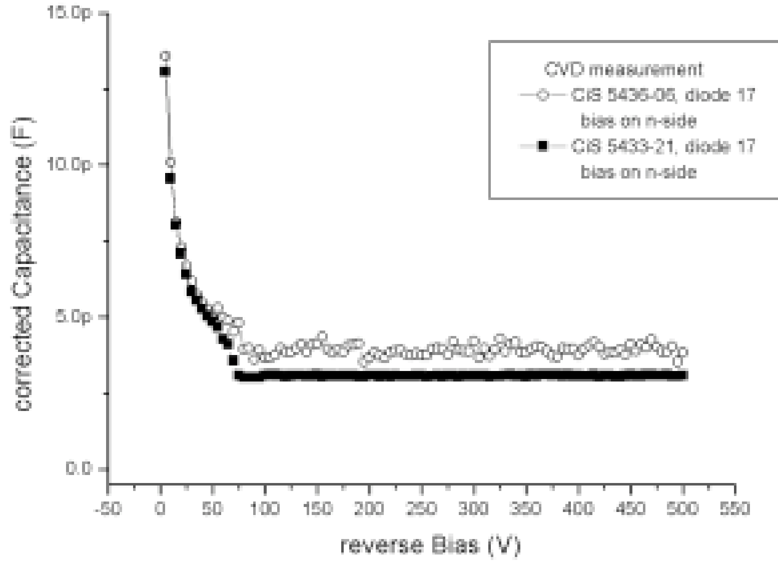


FIG. 12: Capacitance vs. Voltage measurements for production diodes.

Table 3 summarizes the results from the preproduction and production measurements.

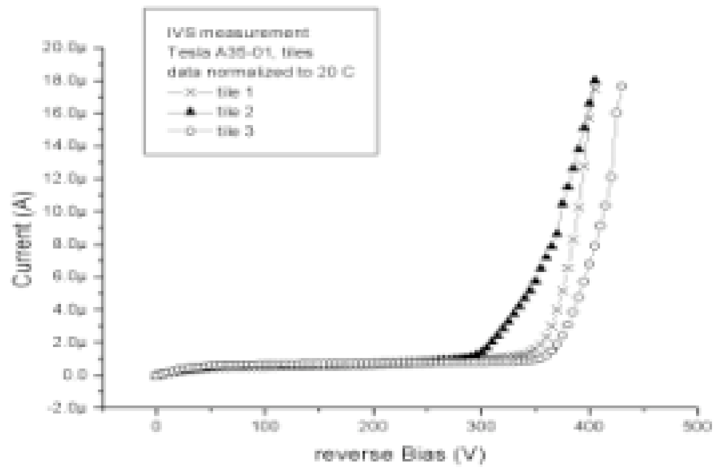
TAB. 3: C-V controls on pre-production and production sensor wafers.In parentheses the total number of wafers is specified.

	preproduction		production
	CiS (14)	Tesla (13)	Cis (84)
$30 < V_{dep} < 120$ V (% good)	100	100	100
2000 Ωcm < ρ < 5000 Ωcm (% good)	100	100	98.8

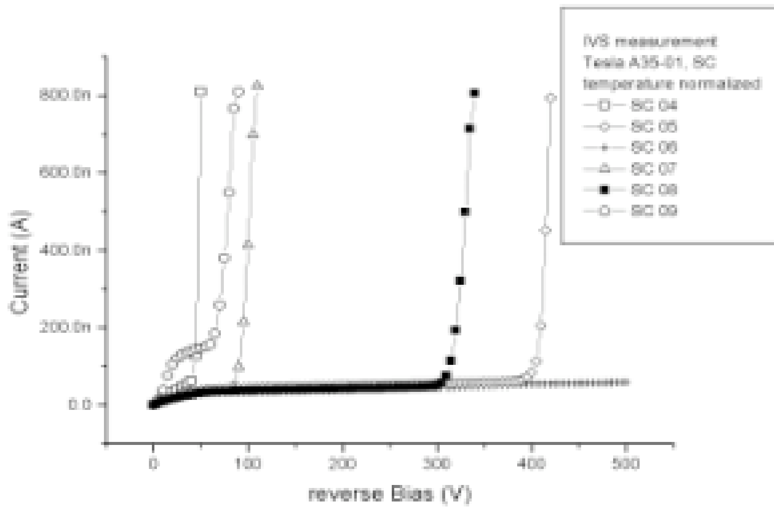
4.2.2 Current-Voltage measurements for tiles, single chips and mini chips

Tiles, single chips and mini chips of all wafers have to be characterized through an I-V measurement; high voltage is stepped through from 0 V down to –500V. The breakdown voltage V_{bd} is defined as the highest measured V with a normalized current I below a set value: $I < 2\mu A$ for tiles, I < 100nA for single chips and I < 25nA for mini chips. Defining I_{op} and I_{50} as the absolute normalized currents at $-V_{op}$ and $-(V_{op} - 50V)$, a current slope is defined as I_{op}/I_{50}. The quality assurance requirements are: $V_{bd} \geq V_{op}$, current slope < 2.

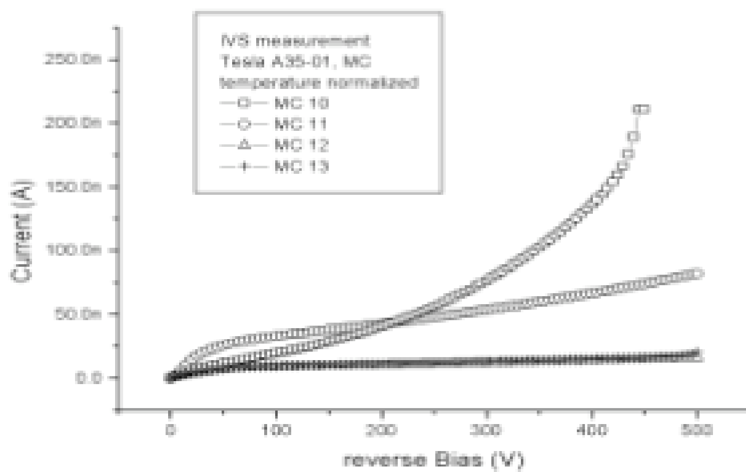
The following plots show some results of I-V measurements taken on tiles, single chips and mini chips respectively, for a selected sub-sample of pre-production wafers. Single and mini chips measurements are not used for wafer rejection.



a

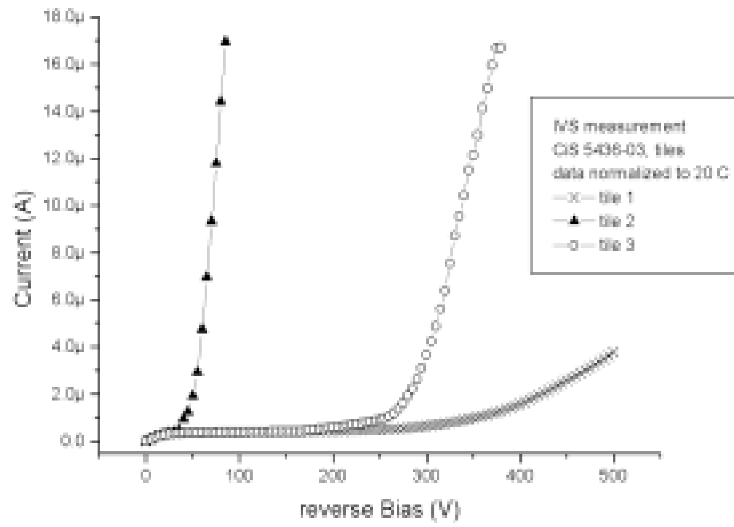


b

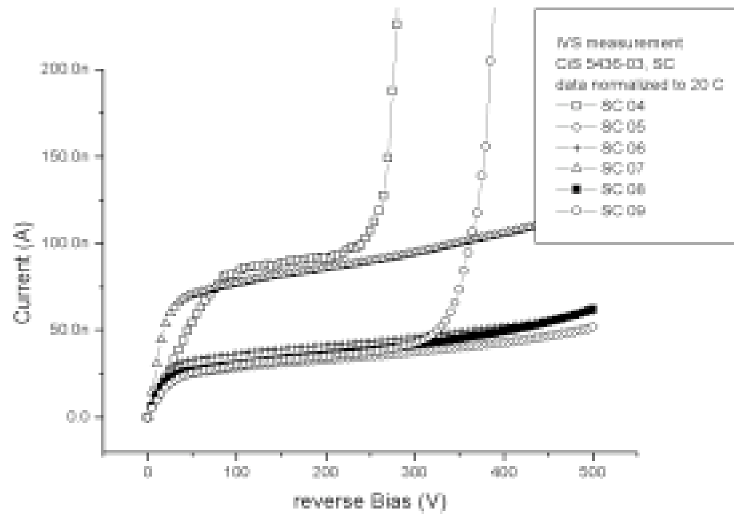


c

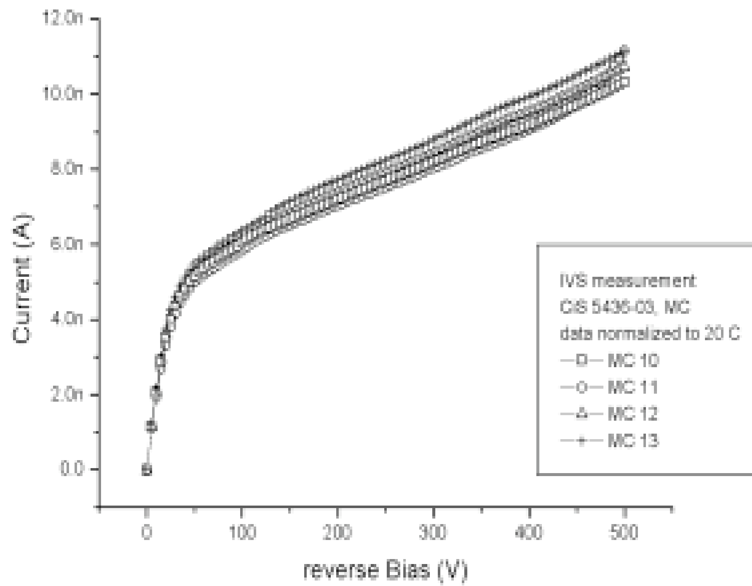
FIG. 13: Current vs. Voltage curves for a) tiles, b) single chips and c) mini chips from pre-production Tesla wafers.



a



b



c

FIG. 14: Current vs. Voltage measurements for a) tiles, b) single chips and c) mini chips from CiS production wafers..

In figure 14 the results of the Current vs. Voltage (I-V) measurements are reported. The measurements have been taken on tiles a), single chips b) and mini chips c) on a selected sub-sample of production wafers. Again, single and mini chips measurements are not used for wafer rejection.

Table 4 summarizes the results on the I-V measurements performed on tiles for both pre-production and production wafers.

TAB. 4: . Number of wafers sorted by the number of good tiles as measured by vendor and our lab on CiS production sensor wafers. Wafers with less than two good tiles are not sent to the labs

# wafers with 3 good tiles	vendor	46
	our lab	44
# wafers with 2 good tiles	vendor	38
	our lab	40

Table 5 summarizes the I-V measurements performed on single chips and mini chips for both pre-production and production wafers.

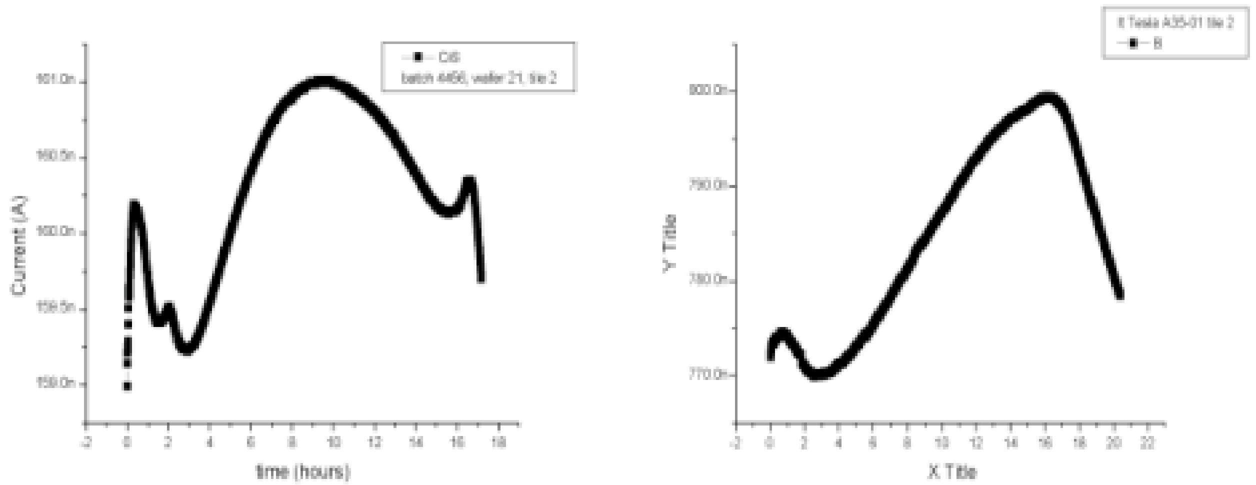
TAB 5: Percentage of good structures for I-V measurements on pre-production and production sensor wafers. In parentheses the total number of single chips and mini chips is specified.

QA criteria	structure	Pre-production		Production
		CiS	Tesla	CiS
$V_{bd} > V_{op}$ & $s < 2$	Single chip	81.1 (84)	58.3 (84)	91.0 (300)
	Mini chip	90.0 (56)	60.0 (56)	91.0 (200)

The strength of the bias grid concept, basically testing all pixels in parallel, is to get a global picture of all the good pixels as well as to be sensitive to any pixel going into breakdown: a heavily damaged pixel implantation will result in a quick breakdown of the entire tile around depletion voltage. Quick breakdowns at a higher voltage can point towards a high and instable field configuration close to a pixel implantation (slow breakdowns usually have other causes).

4.2.3 Tile Current stability over time measurements

It is a QA requirement that the leakage current through the detector be stable over the long time it will be in service. Due to time limitations it is only viable to check few tiles in an overnight measurement. We have therefore reached the compromise to test a good tile on one



randomly chosen wafer from each batch. The high voltage is set to the operational voltage and a current measurement is taken every 10 s for 15 hours. The relevant parameters are the initial and final currents (I_{start}, I_{end}) normalized to 20°C and the current slope I_{end}/I_{start}, which is required to be $\leq$ 1.3. Figures 15 a) and b) show the current, measured at the operational voltage, as a function of time for pre-production tiles; note the very much expanded y-scale. The current values are not temperature normalized, which explains in large part the time variations

FIG. 15: Current vs. time curves for a) CiS and b) Tesla pre-production tiles.

The slope, has been checked to be < 1.3 in 100 % of times for both CiS (4 wafers) and Tesla (5 wafers). Figure 16 shows the same curves for the CiS production wafers. In this case the slope was within requirements for 27 over 28 measured wafers; one wafer was rejected. This measurement is relevant for pixel quality, since quick breakdowns in a time-stability measurement can point towards a high and instable field configuration close to a pixel implantation.

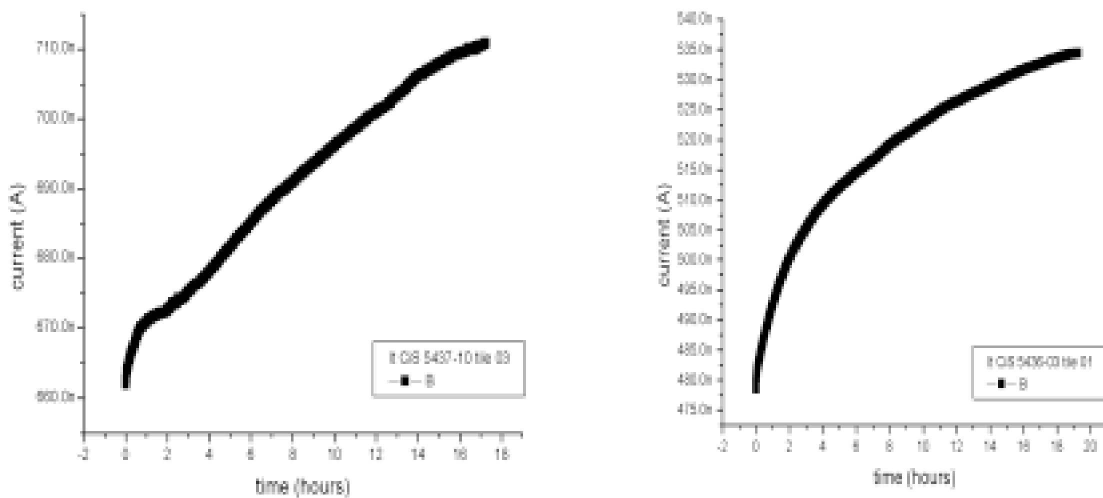


FIG. 16: Current vs. time measurements for CiS production wafers

4.2.4 I-V and C-V on MOS Test Structure

These are batch-based measurements: two wafers are to be measured for each batch.

Silicon dioxide covers part of each pixel and since charge generation at the interface with silicon can give a substantial contribution to the current, it is important to study the oxide properties. The I-V measurement is intended to determine the oxide breakdown voltage, with a required minimum of 50 V corresponding to a limit current of 100 pA. A high current would either mean a surface leakage current along the oxide surface and the edge of the device, or a breakdown of the oxide itself, possibly meaning the destruction of the layer by high voltage. Both cases would point to major problems of wafer processing.

Figure 17 shows examples of I-V measurements for production wafers. All the tested wafers have passed the requirement.

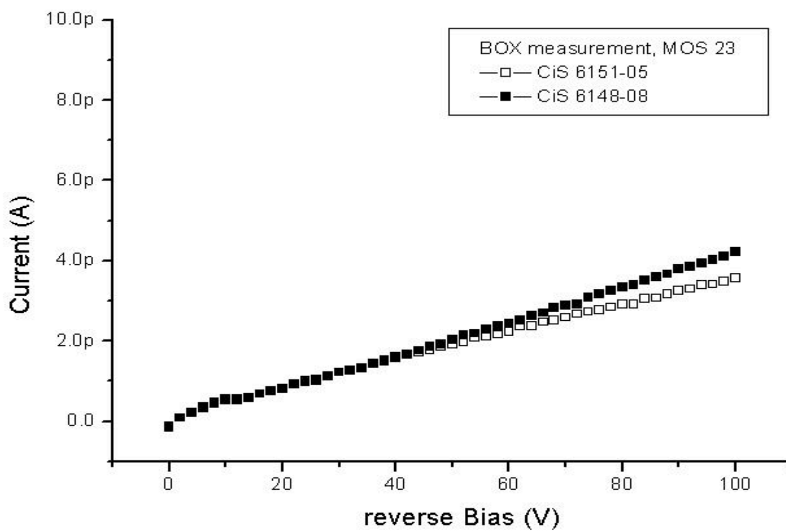


FIG. 17: Current vs. voltage measurements on CiS production oxide test structures.

Capacitance vs. Voltage curves are meant to provide some essential parameters like oxide capacitance, flat-band capacitance and voltage. Typical graphs are shown in figures 18 and 19 for pre-production and production wafers respectively.

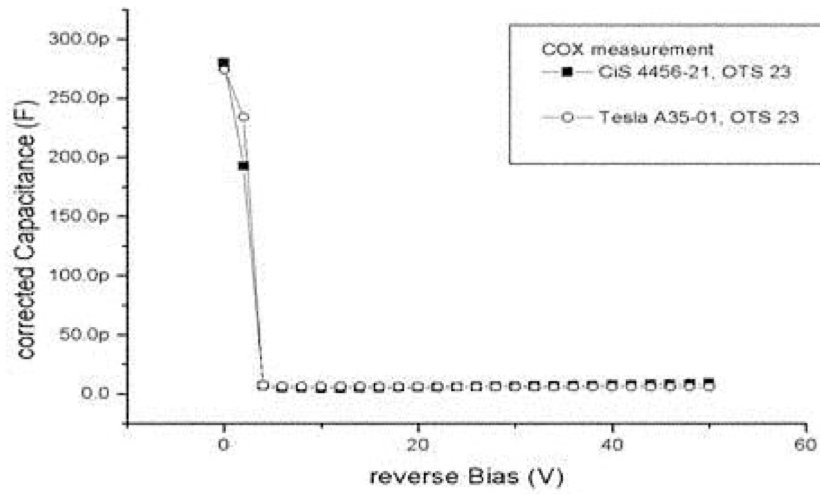


FIG. 18: Example Capacitance vs. Voltage measurements on oxide test structures for pre-production wafers

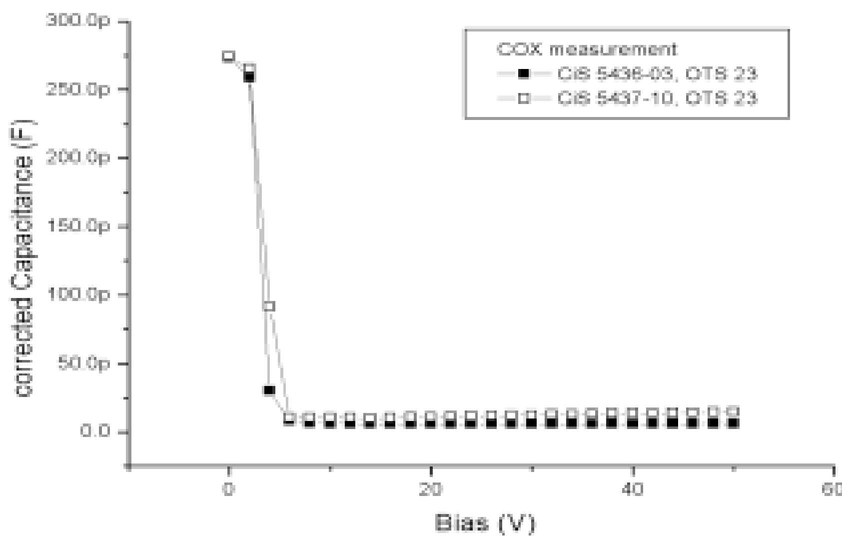


FIG. 19: Capacitance vs. Voltage measurements on CiS production oxide test structures.

4.2.5 I-V_{gate} on gate-controlled diode

This is a batch-based measurement: two wafers are to be measured for each batch.

The current measurement is meant to determine the oxide interface current. The difference between the current at the last measured voltage before the interface generation current rise (flat band voltage: V_{FB}) and the current measured at the last measured voltage before the current flattens to a new plateau, is an approximation of the interface generation current.v

Figures 20 and 21 show the distributions obtained for the I-V_{gate} measurements performed on pre-production and production wafers respectively.

This measurement can detect possible additional currents from the interface into the pixels if the flat-band voltage is relatively low.

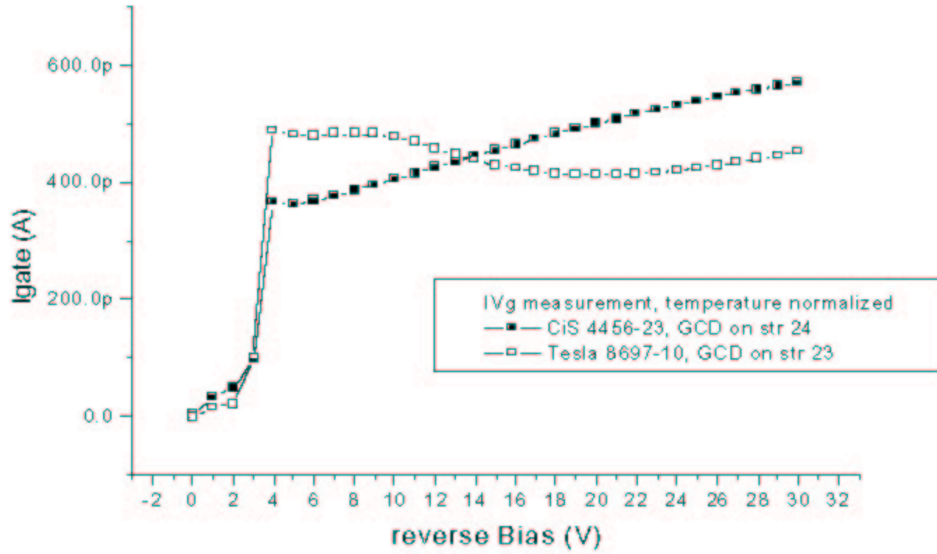


FIG. 20: Current vs. gate voltage measurements on pre-production diodes.

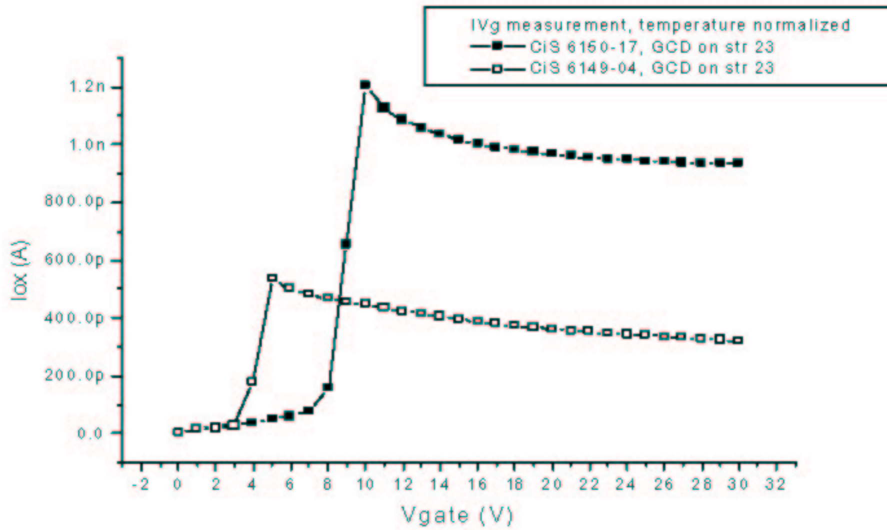


FIG. 21: Current vs. gate voltage measurements on CiS production diodes.

4.2.6 I-V_{gate} on MOSFET

This is a batch-based measurement: two wafers are to be measured for each batch. The source-drain current as a function of V_{gate} is measured, to derive the p-spray dose. From the last measured voltage before the source drain current rise (threshold voltage V_{thr}), one can estimate the p-spray dose, which is requested to be $2.5 \cdot 10^{12}$ < p-spray dose < $3.5 \cdot 10^{12}$. V_{thr} is

requested to be >0. For pre-production wafers, this measurement was done starting June 2002, that is only for Tesla wafers and only on six of them. All passed the test.

The measurements performed on the MOSFET structures are reported in figures 22 and 23 (for pre-production and production wafers respectively). All production CiS batches (for a total of 36 selected wafers) passed the test.

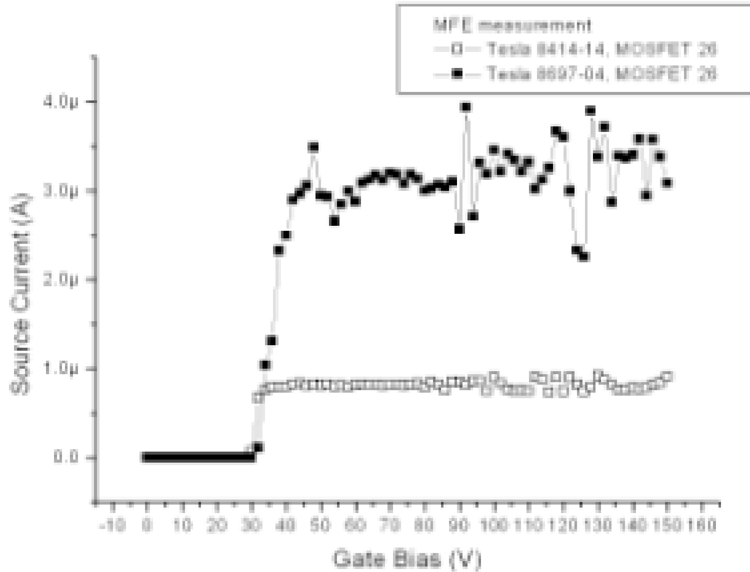


FIG. 22: Current vs. Voltage on MOSFET structures for pre-production Tesla wafers.

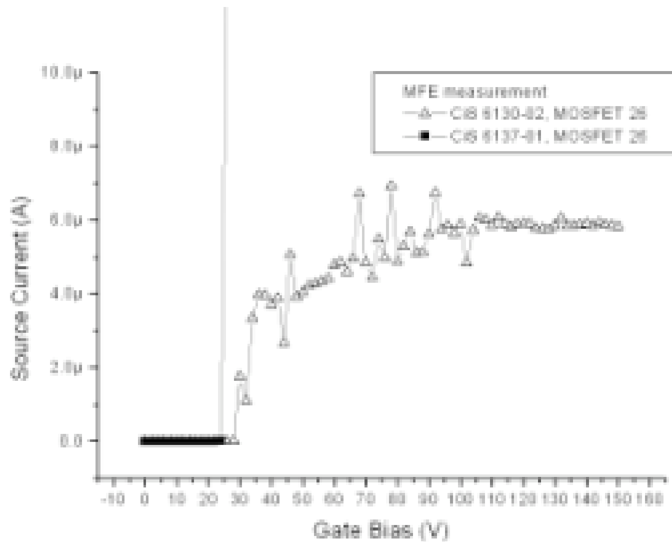


FIG. 23: Current vs. Voltage on CiS production MOSFET structures.

Since pixels are fabricated on the n-side of the detector, they would be shorted by the electron layer present at the Si-SiO_2 interface, unless a p-type layer is created between them. This measurement is relevant in assessing the quality of such an isolating layer.

4.2.7 V_{pix} on punch-through structure

This is a batch-based measurement: one wafer is to be measured for each batch.

A bias grid is present on tiles and is meant to bias pixels via a punch-through mechanism. It allows pixel electrical testing prior to the electronic chip bonding and pixel grounding in case bonding fails. The punch through voltage at the operating voltage is required to be ≥ 3V. Typical distributions are shown in figure 24 for pre-production wafers of CiS a) and Tesla b) respectively.

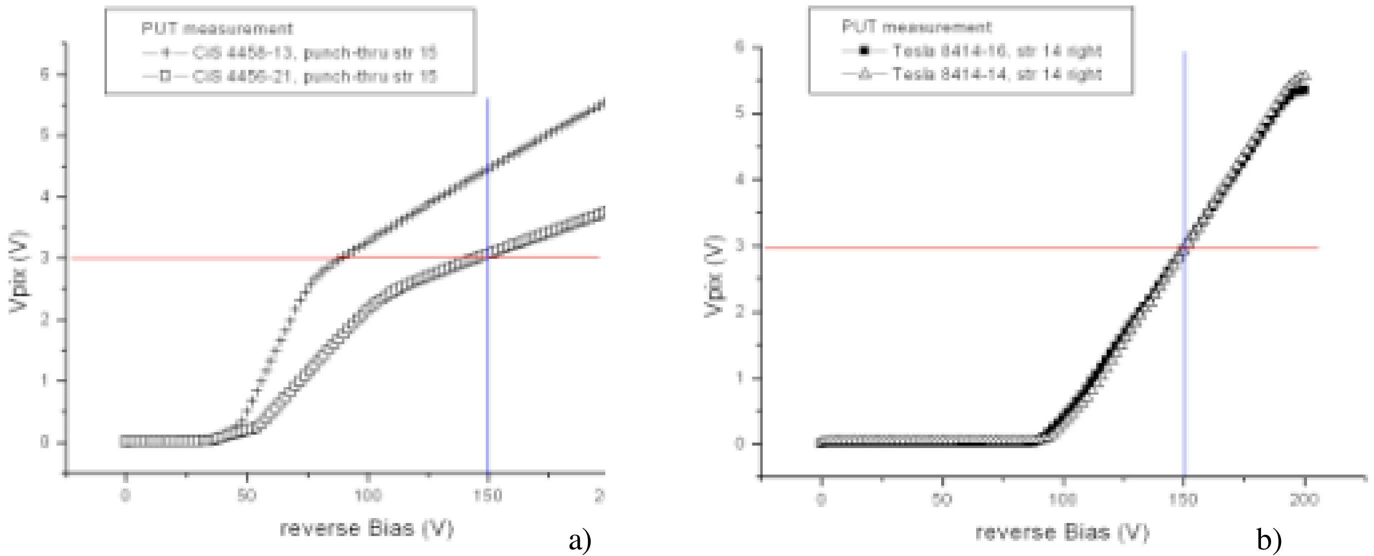


FIG. 24: Punch through Voltage for Tesla (a) and CiS (b) pre-production wafers.

For CiS pre-production 3 of 3 batches satisfied the QA criteria, while 1 wafer did not. For Tesla pre-production 2 of 4 batches and a total of 4 wafers did not satisfy the criteria. Figure 25 shows the same distribution for CiS production wafers. In this case the criteria was satisfied by all 27 measured batches, even though 2 wafers did not pass the test. One of these wafers also had a visual inspection non-conformity, both were rejected. This measurement is not only important to know the potential drop across the bias dots during grid biasing. It also makes a statement about the potential deviation in non-contacted pixels after bonding and it gives additional information on the properties of the p-spray layer especially concerning the effects of misalignments of the implantations and the depth of the p-spray channel.

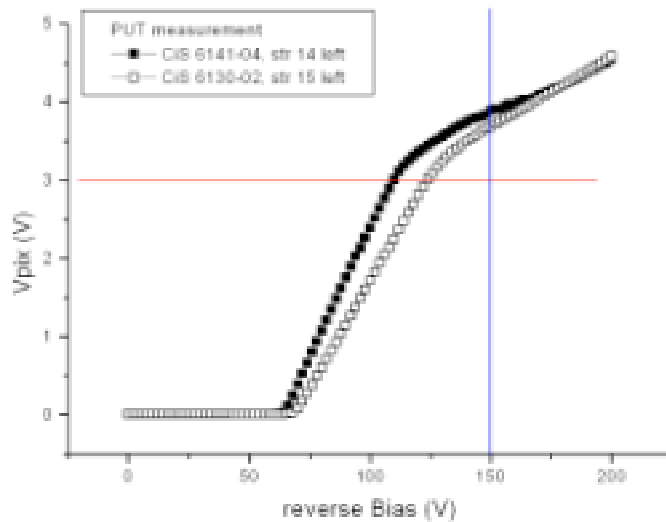


FIG. 25: Punch through Voltage for CiS production wafers.

5 FUTURE PLANS

The Quality Assurance tests on the wafer sensors for the ATLAS Pixel detector at the Udine Silicon laboratory is now well established and under control, thanks to the financial support of the Istituto Nazionale di Fisica Nucleare – Gruppo Collegato di Udine, and of the University of Udine.

The whole production expected from CiS has been already delivered to the laboratory and measurements are undergoing. Starting from March 2004 we are expecting the delivery of production wafers from Tesla: we are confident to fulfil our commitments within the scheduled time.

6 ACKNOWLEDGEMENTS

We gratefully acknowledge Jonas Klaiber-Lodewigs' help in clarifying the measurements procedures and their relevance to pixel quality.

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