

INFN-17-03/GE
2nd March 2017

The High Voltage Regulator Board for the BDX Experiment

Andrea Celentano, Massimiliano Cresta, Giuseppe Minì, Giacomo Ottonello,
Fabio Pratolongo

INFN, Sezione di Genova, Via Dodecaneso 33, I-16146 Genova, Italy

Abstract

In this note we describe the design and construction of SiPM High Voltage (HV) Regulator board for the BDX experiment. The board is used to provide bias voltage to the Silicon PhotoMultipliers (SiPMs) used in the BDX detector. It hosts four independent channels, each with a selectable output voltage in the range 37 V to 80 V: each channel is individually regulated by means of a variable resistor.

In the note, after a brief introduction to the BDX experiment, we present the design of the board, discussing in particular the critical aspects that we identified during the circuit implementation phase. We also show the results obtained from the characterization of a first sample of 10 boards.

1 The BDX experiment at Jefferson Laboratory

The “Beam Dump eXperiment” (BDX) (1) is an e⁻ beam, thick-target search at Jefferson Laboratory for Light Dark Matter (LDM) in the mass range $10 \div 1000 \text{ MeV}/c^2$. BDX will detect dark matter particles produced by the primary e⁻ beam impinging on the JLab Hall-A beam dump, by measuring the scattering on a detector placed about 20 m downstream. The BDX detector will measure both χ - nucleon and χ - electron scattering. These two reactions have a very different signature in the detector: MeV nucleon recoil vs. GeV EM shower. Thus, the sensitivity to both is a powerful handle to control systematics.

The BDX detector is a segmented homogeneous calorimeter, made by CsI(Tl) crystals formerly used in the end cap BaBar Ecal, with an improved SiPM-based readout. Each SiPM is coupled to a custom trans-impedance amplifier, that also provides the bias voltage to the photo-detector. The calorimeter is made of about 800 crystals, resulting in a 0.5 m^3 active volume. The crystals are arranged in a sequence of arrays, each 30 cm long. In order to suppress cosmogenic and beam-related backgrounds, the calorimeter is surrounded by two active-vetoes, made by plastic scintillator layers read by PMTs and SiPMs. Between the inner and the outer veto, a 5cm thick lead vault shields the calorimeter from low energy photons. The detector will be placed about 8 m underground, in a new experimental hall, in order to shield it from cosmogenic particles and also to match the depth of the Hall-A beam dump. To shield the detector from beam-related backgrounds, about 10 m of concrete and iron will be placed between the beam dump and the new hall.

The detector concept has been validated by a measurement campaign at INFN - Sezione di Catania and Laboratori Nazionali del Sud (LNS), performed with a small-scale prototype (2). The prototype was equipped with a single CsI(Tl) crystal, read by two $3 \times 3 \text{ mm}^2$ SiPMs (Hamamatsu S13360-3025CS and S13360-1350CS), with pixel size of 25 and 50 μm . Both sensors were coupled to the same trans-impedance amplifiers foreseen in the final design. The high voltage for the two SiPMs, as well as the bias voltage for the amplifiers, was provided by a custom designed board (the HV regulator board), with an on-board variable DC-DC converter, working with +5 V input voltage. The crystal was surrounded on all sides by a layer of veto detectors (Inner Veto or IV), a vault of lead bricks, and a second layer of veto detectors forming the Outer Veto (OV).

2 BDX HV Regulator Board

The HV regulator board is designed to provide bias voltage to the SiPMs used in the BDX calorimeter and in the active-veto systems. The board has four independent output channels, each with a programmable output voltage in the range 37 V – 80 V, matched to the SiPM working point. Each channel couples to the trans-impedance amplifier used to read the SiPM signal, and also provides the necessary +5 V and -5 V voltages to the amplifier.

The board has been designed by the INFN-Genova electronic group. The key component is an on-board programmable DC-DC converter, working with +5 V input voltage

(LT3482 by Linear Technology (3)). The detailed schematic of the HV Regulator Board is shown in Fig. 1.

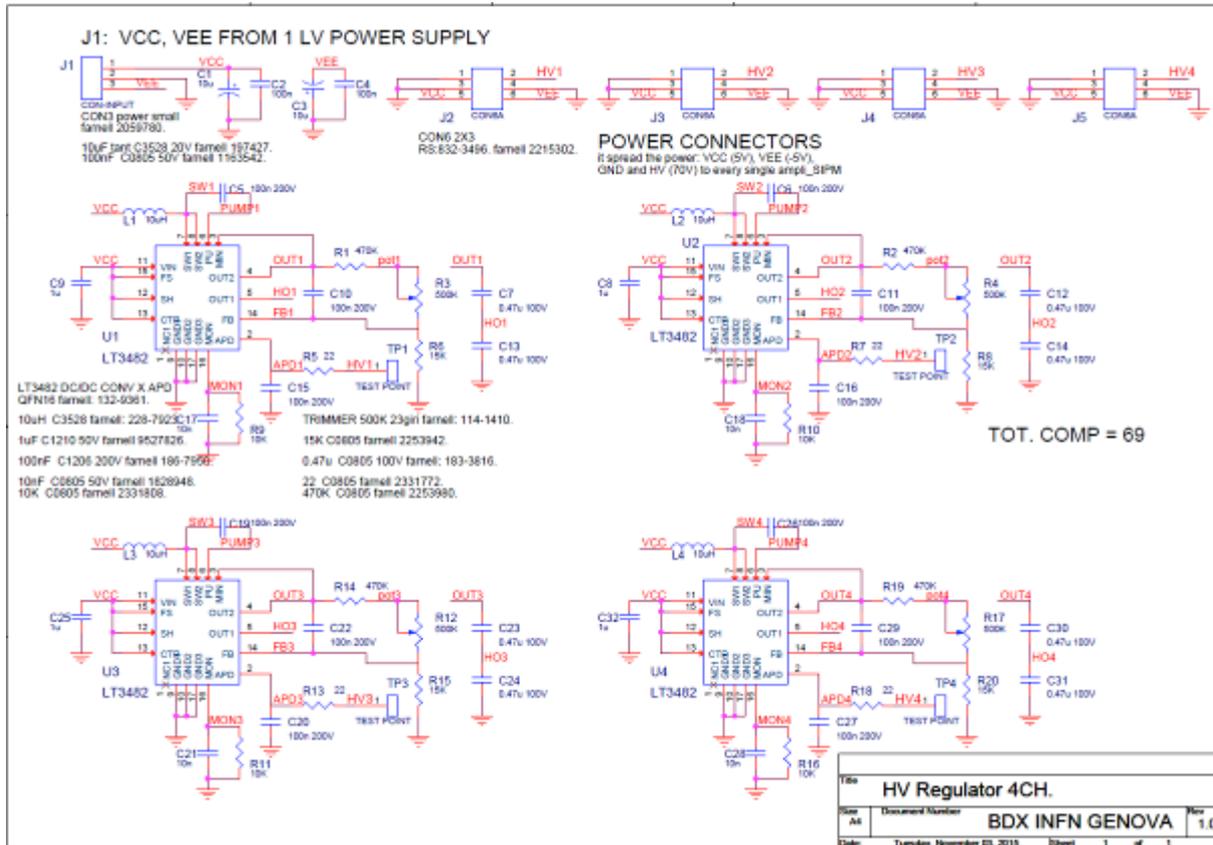


FIG. 1: Schematic of the board.

The LT3482 is a fixed frequency current mode step-up DC/DC converter with voltage doubler designed to bias avalanche photodiodes (APDs) in optical receivers, that can provide up to 90V at the output. The LT3482 is available in a small footprint (3mm × 3mm) 16-lead QFN package, thus allowing a compact design solution. The integrated power switch, Schottky diodes and APD current monitor allow a low-cost solution.

The LT3482 converter is based on a constant-switching frequency solutions, that result in a predictable output noise level, that can be easily filtered. The inductor-based topology ensures an input free from switching noise. The integrated high side current monitor produces a current proportional to APD current with better than 10% relative accuracy over four decades of dynamic range in the input range of 250nA to 2.5mA. This current can be used as a reference to provide a digitally programmed output voltage via the CTRL pin.

In the current board design, the output voltage value for each channel is tuned trough a variable resistor. Using as reference channel 1 in the board schematic, the corresponding output is given by the equation:

$$V_{out} = V_{ref} * (1+(R1+R3)/R6)$$

where V_{ref} is the internal voltage reference value of the DC/DC converter (1.235V), and R_3 is the actual value of the variable resistor. The design solution that has been implemented foresees a series made by a fixed resistor (R_1 , 470k) and a variable one (R_3 500k), resulting in large range of variability for the output voltage, approximately between 37 V and 80 V.

The noise associated with an external switching power supply can affect the output voltage provided by the board. To suppress this noise, a $0.1\mu\text{F}$ capacitor has been added at the output pin. An additional output low pass filter, made by a 10k resistor and a 10nF capacitor, has been implemented at the MON pin, to further reduce the power supply noise and other wide band noise. Other ancillary components used in the project and coupled to the LT3482 DC/DC converter are those suggested by the manufacturer (3).

The four output connectors (J_2, J_3, J_4, J_5) are simple flat connectors 2.54 mm pitch, 6 pin trough all, that carry the HV signal, the +5 V and -5 V voltages and the ground reference to the SiPM amplifiers. Power for the HV regulator board (+5V and -5V) is provided through a single input connector (J_1). A picture of the full PCB with all the 69 components assembled is shown in Fig. 2.

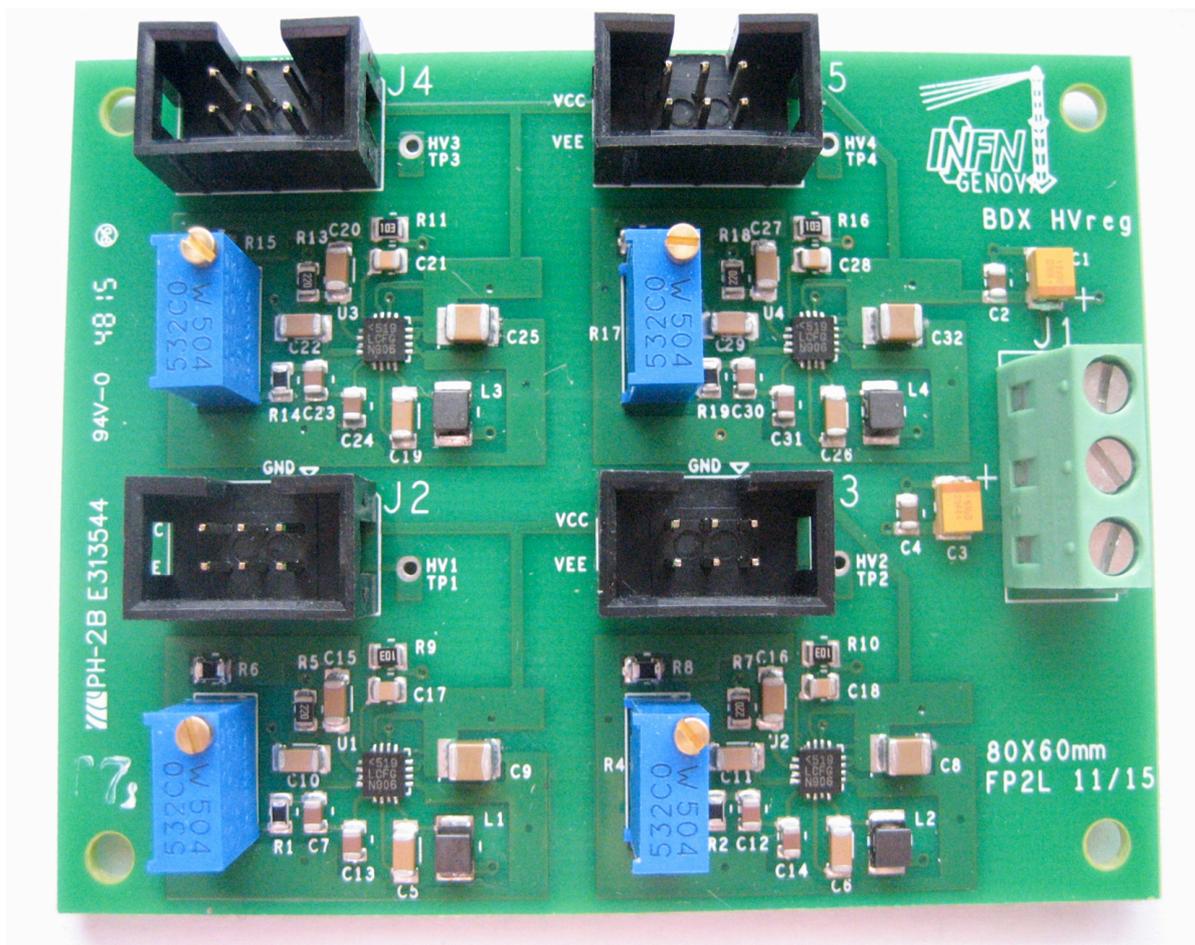


FIG. 2: HV Regulator board.

While Fig.3

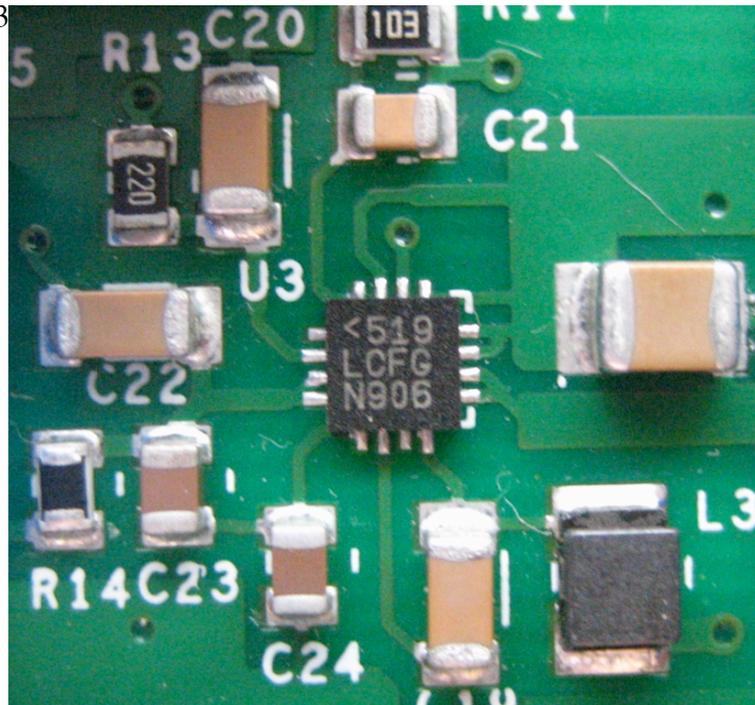


FIG. 3: zoom in the U3 zone.

3 HV Regulator board layout

The layout of the HV regulator board is critical, because of the LT3482 reduced package (QFN, 16 pins), that also foresees a central pad that has to be connected to the ground plane, thus requiring a very precise PCB design and a careful alignment during mounting operations (a detailed view of the PCB design for the LT3842 component is shown in Fig. 4)

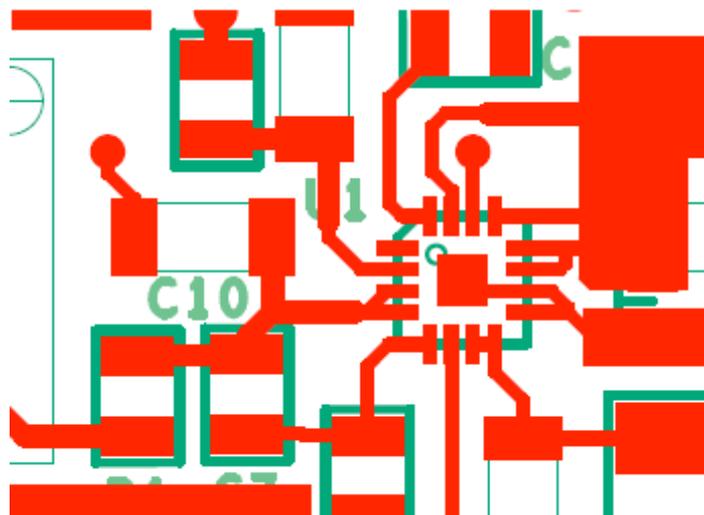


FIG. 4: U1 routing on TOP layer.

In order to validate the design, before proceeding to a larger production, we made a board prototype, equipped with two channels instead of four, to check the feasibility of the circuit and the layout. The circuit, shown in Fig. 5, was constructed using the milling cutter tool of the INFN-Genova electronic service.

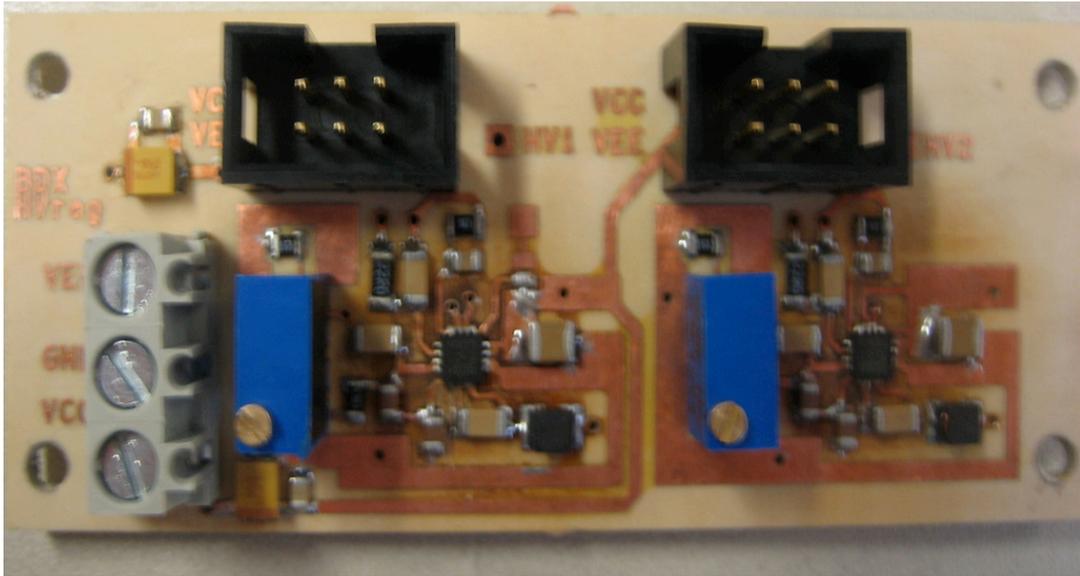


FIG. 5: board prototype.

After the prototype experience, that was particularly helpful to understand how to design the nets around the LT3482, we proceeded to design the final circuit, following the manufacturer specifications closely.

The final board design is a 2-layers PCB (FR4 material), 80x60 mm, with 69 components, and a standard thickness of 1.6 mm. Most of the traces routing is performed on the TOP layer, while the BOTTOM layer is dedicated to the ground plane. The design rules we adopted were: 0.3 mm width for nets and 0.5 mm widths for supply with a minimum spacing of 0.3 mm. Figure 2 shows the picture of the PCB with the assembled components, while Figure 4 shows a detail of the routing on the TOP layer, around one of the DC/DC converters.

4 Board performances

A small pre-production series of 10 boards has been made, in order to verify the reproducibility of the performances. In particular, after verifying each channel was working properly, we measured the minimum and maximum output voltage values, thus determining the dynamic range. Fig. 6 and 7 shows results for the first 5 boards (20 channels in total).

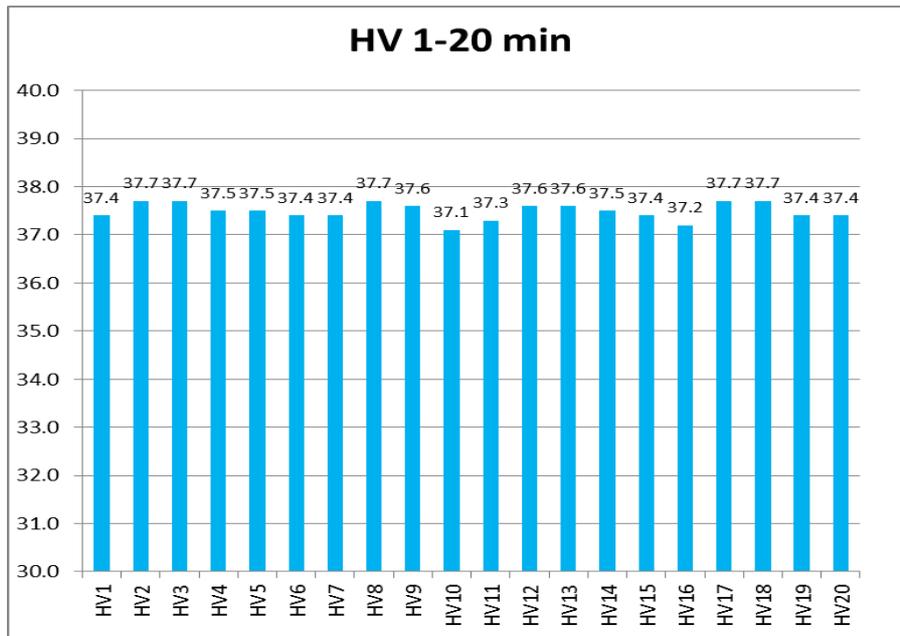


FIG. 6: HV minimum for first 20 outputs.

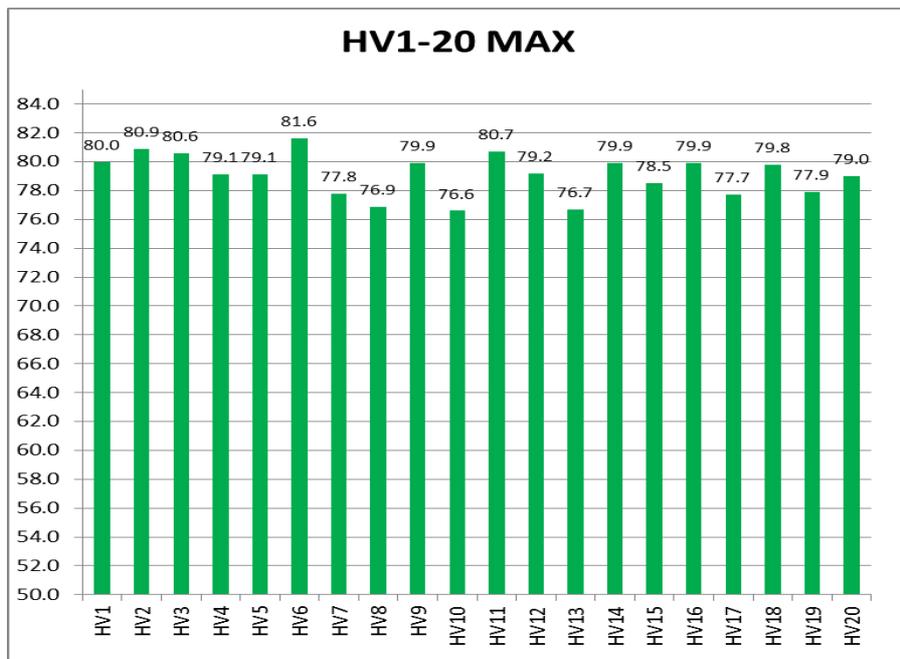


FIG. 7: HV maximum for first 20 outputs.

All minimum values are between 37 V and 38 V, while maximum values range between 76.6 V to 81.5 V: these results are compatible with the tolerances on the mounted components, and thus confirm the validity of the chosen design. The same results were found for the other 20 channels.

We also evaluated the stability of the output voltage value by testing few channels. We fixed the value of the output voltage close to 65 V (typical value of the working point of SiPMs used in the BDX detector), and we measured it every hours, for a time interval of two days. Results are shown in Fig. 8, and demonstrate that the stability of the system is better than 99.9 %. In the same way we controlled other output voltages of other boards always finding excellent stability. The boards performed well and all the specifications were met.

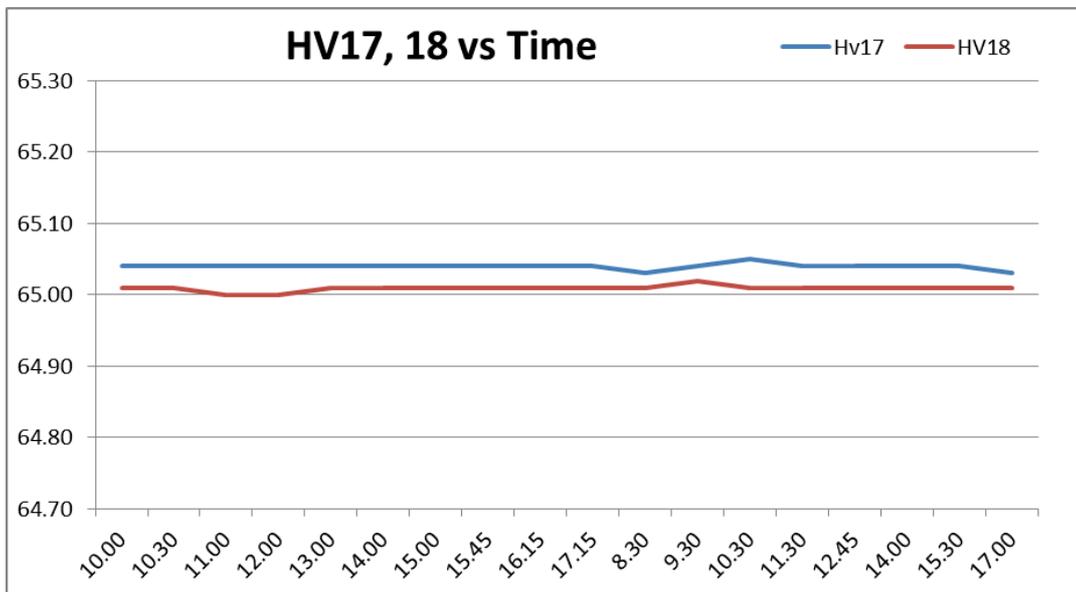


FIG. 8: HV17 and HV18 versus time.

5 References

- (1) A.Celentano "Dark sector searches at Jefferson Laboratory".
- (2) The BDX Collaboration, "Dark matter search in a Beam-Dump eXperiment (BDX) at Jefferson Lab".
- (3) Linear Technology, "90V Boost DC/DC Converter with APD Current Monitor".