ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Genova

INFN-17-01/GE
18th January 2017

Implementation of a New Electronic Trigger for Borex @ Lngs

Massimo Cariello

INFN, Sezione di Genova, Via Dodecaneso 33, I-16146 Genova, Italy

Abstract

To adapt signals between the new trigger board and the DAQ of borexino experiment it was necessary to implement an interface board to deal with a large number of signals at different logic levels.

Pubblicato da SIDS–Pubblicazioni
Laboratori Nazionali di Frascati

Presented at the Borexino-SOX General Meeting (Milan 14/12/2016 – 16/12/2016)

1 WHY REPLACE THE OLD TRIGGER

The problems that have occurred during the data-taking in BOREX have even more highlighted the need to provide for the implementation of a new electronic trigger. The main cause is a problem of start-time that had already manifested during BOREXINO phase 2 and it is caused by the old trigger board (BTB) which sometimes produces a jitter of the position of the events within the DAQ gate. Deformation of the event cluster affects the energy reconstruction at low energies and it causes that normal events were rejected as bad.

BTB board was substituted with spare in April 2015 to fix the same type of problem. Now we do not have any more spares, and the troubles we are once again experiencing with the start-time have made it urgently necessary to replace the trigger system with a new one.

FIG. 1: Previous Trigger System.

2 HOW IT WAS MADE

The choice was not to build a complex custom board but to use a programmable card on the market, the V1495 of CAEN, according to the standard VME already in use, exploiting to the full all its versatility and achieve parallel card interface, this also according to the standard VME, that is able to adapt the multifaceted BOREX environment with the high density connectors and the LVDS standard of the V1495.

As shown in Figures 1 - 2 - 3 the intervention is to change the software of PPC (Power PC), a small change in the hardware of the Clock Generation Board (which becomes only distribution), the elimination of cards BTB (BOREXINO Trigger Board) and Tab5 (that sums

the results), the inclusion of the V1495 that takes care of the generation of the trigger and the Interface Board that deals with all the signals involved.

FIG. 2: Trigger System now.

3 INTERFACE BOARD

Fig. 4 shows the signals managed by the interface board and the logic levels used, now let's see in detail how they were implemented.

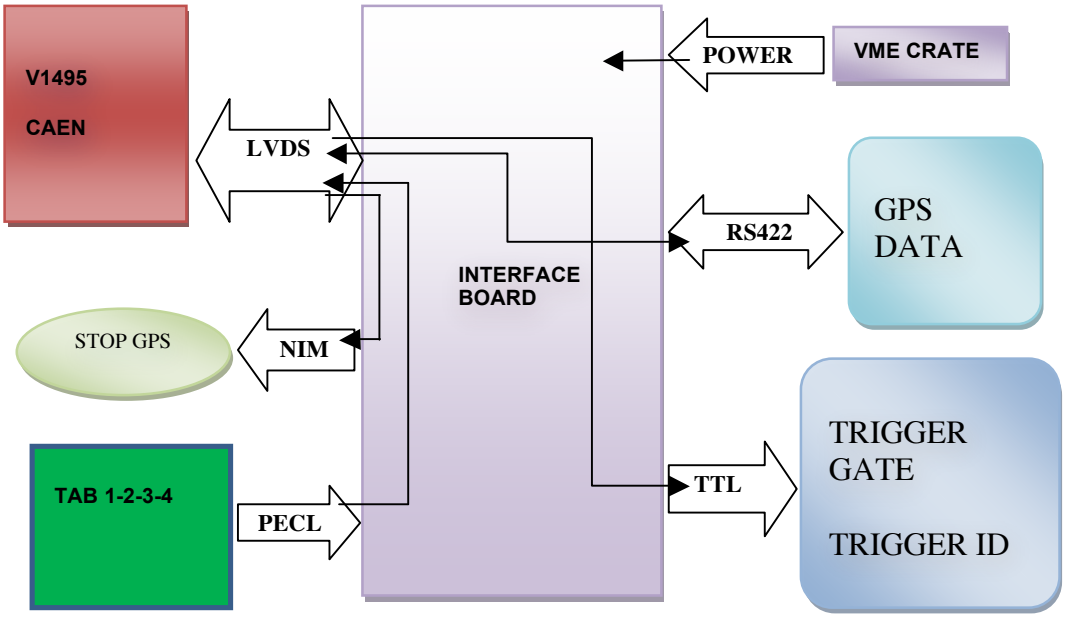

FIG. 3: Interface Board Block Diagram.

The connection to the V1495 card is realized through 3 high-density connectors Robinson 68 pins; two for the signals that coming out of the Interface Board (Conn A J3 and Conn B J4 – LVDS output) and one for the signals entering the Interface Board (Conn C J5 – LVDS input). These, combined with the Lemo connector dedicated to the signal STOP_GPS (NIM out) and the LEDs for power on, take up all the available space on the front panel of a 6U board size, then force us to adopt an additional card (Piggy Board) that can accommodate the other connectors required. Piggy Board hosts 4 header connectors 26pins that receive signals sum of Tab 1-2-3-4 (PECL input) and has also space available for some spare connectors. In the back of the Interface Board connectors take place in accordance with the standard VME: P1-J1 and P0-J0 are only used for the power supply voltages (Ground, + 5V and -5V) while P2-J2 connector is customized and exchanges the data with the GPS system (RS422 input and output) and the Fan-Out card which distributes the signals of the trigger (TTL output). All this in compliance with the old BTB board.

To provide the signals in LVDS format to the V1495 card is used the MAX9180, a low-noise LVDS repeater, single channel and low supply current, this has allowed to optimize the power dissipation and to easily maintain the same delay times in all signals involved. The conversion, both for PECL signals from TABs card and for RS422 signals from the GPS, is obtained by a resistive divider which precedes the repeater.

The opposite conversion from LVDS to TTL is made with the quad differential line receiver DS90C032. This is enough for trigger signals that go toward the fan-out, while the signals that go to the GPS are further converted into 422 by the quadruple differential line driver AM26C31 or as regards the STOP-GPS in NIM by a simple operational stage as a current amplifier with the AD8014.

4 ABOUT THE SCHEMATICS

The project was developed with Cadence software (Allegro Design Entry CIS v16.6), the files are available in the electronic-service working area of the Genoa section.

The scheme has been designed thinking about the possibility of some upgrade during the two years of SOX data acquisition; for this reason, each unused pins of the connectors used was made available for future use and some interface ports were mounted even if for the moment are not used. That way if it will take new signals will not need to build a new PCB, but simply necessary to program the new releases and connect some pins.

The details of the schematic can be downloaded at:

https://www.ge.infn.it/~cariello/borexino/interfaceboard.pdf

https://www.ge.infn.it/~cariello/borexino/piggyboard.pdf

5 PRINTED CIRCUIT BOARD AND COMPONENT ASSEMBLY

The two printed circuit boards (interface and piggy) are both six layers, they have been made on a single panel of material so as to optimize costs. For the same reason it was decided to proceed independently for the mounting of components. Fig.4 shows the two PCBs assembled.

Top view of the two PCB can be found at:

https://www.ge.infn.it/~cariello/borexino/PCB_InterfaceBoard.pdf

https://www.ge.infn.it/~cariello/borexino/PCB_PiggyBoard.pdf

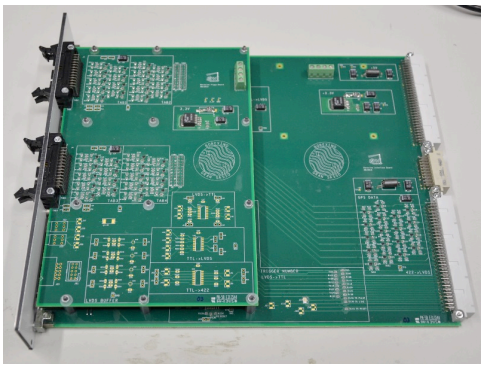

FIG. 4: Interface Board Assembled.

In the last it has been also designed the front panel (Fig. 5) that gives a professional look to the assembled board, made in “Alupanel”, a compound of two aluminum thin laminated together by a plastic polymer for a total thickness of 3 mm.

FIG. 5: Front Panel View.