# ISTITUTO NAZIONALE DI FISICA NUCLEARE

**Sezione di Genova**

# THE ELECTRONIC DESIGN AND THE LAYOUT OF CENTRAL LOGIC BOARD (CLB) FOR THE KM3NET EXPERIMENT

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## Abstract

In this note we describe the design and construction of Central Logic Board (CLB) for the KM3NeT experiment. This board is inserted into the Digital Optical Module (DOM). The CLB is designed to manage slow control instrumentations and PMT data for each DOM. An optical connection is used to receive commands and send all the data to the On Shore station.

# 1    KM3NET EXPERIMENT

KM3NeT is a future European research facility in the Mediterranean Sea that will house a neutrino telescope of cubic kilometer scale. Cherenkov light from neutrino-induced secondary particles will be detected by an array of Digital Optical Modules (DOM) consisting of high pressure resistant glass spheres hosting photomultipliers inside. This vessel is called the DOM and it is composed of 31 small 3 inch photomultipliers (PMTs) distributed around the glass sphere, which collects the Cherenkov photons and transforms them into electronic signals. The PMTs are suspended in a foam support structure: 19 in the lower hemisphere and 12 in the upper hemisphere. Each PMT has its own adjustable high voltage supply integrated in the PMT base.

In addition to the PMTs the DOM contains the Central Logic Board (CLB), which converts the electronic signals from the PMTs into time, pulse duration and identification information in the Time To Digital (TDC) core embedded in the Field Programmable Gate Array (FPGA) of the CLB. The data provided by the PMT bases are collected and distributed to the CLB by means of two boards, the so called Octopus Boards. All necessary DC power is provided by the Power Board (PB) (1).

# 2    CLB DESCRIPTION

The Central Logic Board version 2 is an evolution of the previous CLB version 1 used in the project of ANTARES; starting from this, an upgrade and an optimization were made, with these main differences:

- The FPGA is now embedded on the board.
- CLB uses the White Rabbit Protocol for time synchronization.
- The instrumentation is embedded on the board.
- The data are transferred using an SFP transceiver, instead of the REAM.

The CLB is a board based on a FPGA Xilinx Kintex 7, which is connected with all the electronics inside the DOM, to acquire the data from PMTs with Octopus connectors, send them via fiber optics to the ground station, and allow a remote control of instrumentation. A block diagram with all the main elements present on CLB is shown in figure 1.

The CLB integrates the White Rabbit Protocol (5) (White Rabbit is a fully deterministic Ethernet-based network for general purpose data transfer and synchronization), which allows to synchronize the all KM3NeT DOMs within 1 ns resolution.

The Embedded instrumentation on CLB are the Attitude Heading Reference System (AHRS) chip which provides information on Tilt and Compass and the SHT21 which provides information on Temperature and Humidity.

AHRS integrates the data coming from accelerometers, gyros, magnetometers, using a sensor fusion algorithm, based on Kalman Filtering techniques, running on a high performance high-speed digital signal processor to provide a complete 6 DoF attitude. The detailed information on this chip are in (3).
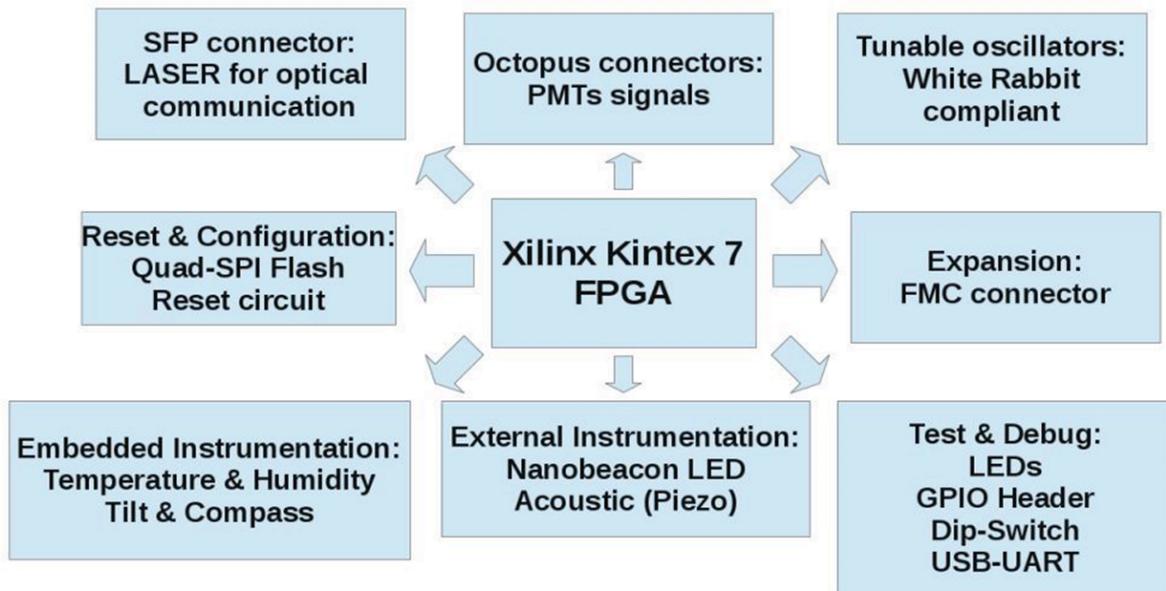


**FIG. 1:** A block diagram with all CLB elements.

In addition CLB manages, acquires data and sends them to the ground station from instruments outside of the board as the Nanobeacon and Acoustic device.

The CLB uses a SFP module with its electronic and photonic components for an optical serial link to the shore.

Finally, in the CLB there are the reset circuit and the configuration circuit. Additional connectors for test and debug of the board are present and they were used intensively in the prototype phase. These tests involved the group of Genova but also other laboratories as IFIC in Valencia, NIKHEF in Amsterdam and INFN Bologna. The results are good and meet the specifications requested by the collaboration. For more details on all the performed tests on the CLB refer to (4).

The CLB version 2 is shown in figure 2.
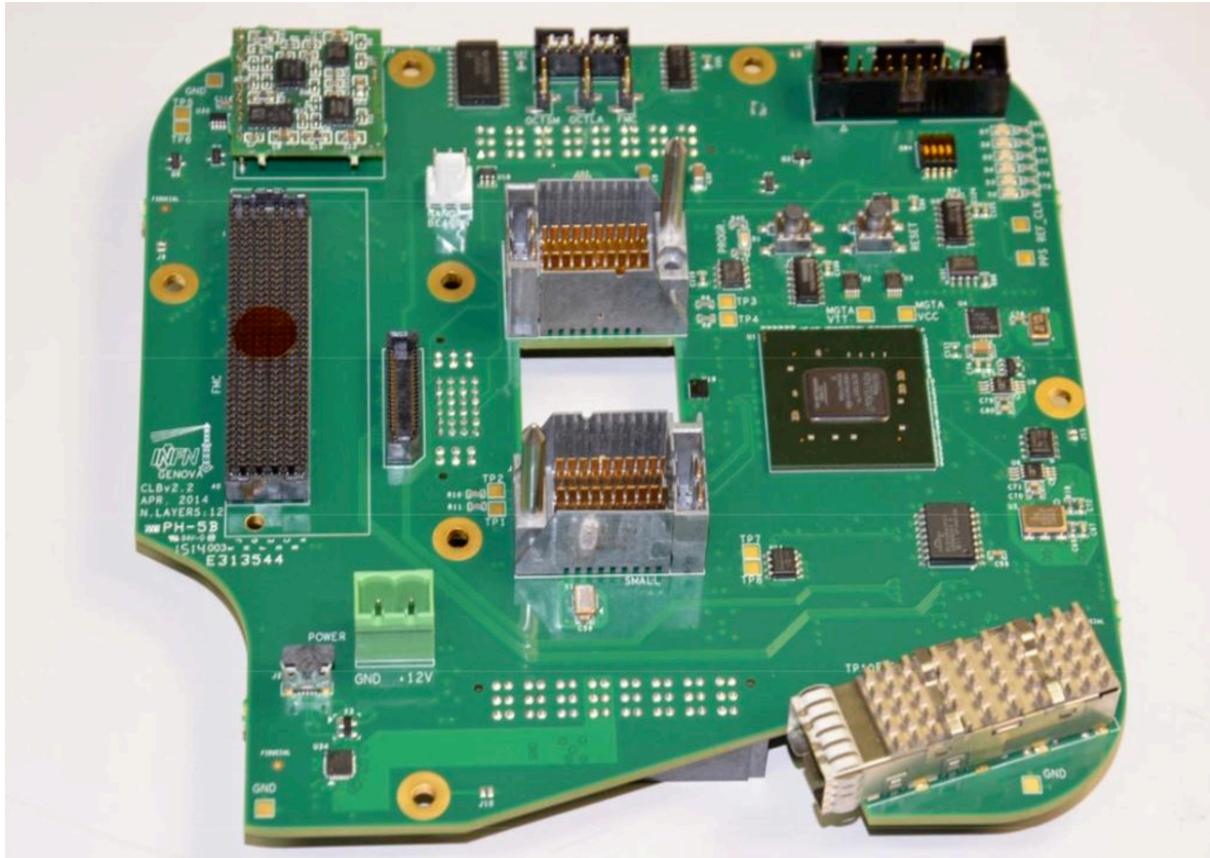
**FIG. 2:** A picture of the CLB.

## 3    CLB DESIGN

The schematic of the Central Logic Board has been designed using the software Orcad Capture, and consists of 14 sheets in A3 format. The first two pages are informative, presenting a block diagram of the general board, with references to the sheets of the schematic and the FPGA banks. Moreover, the JTAG chain, the power supplies used on the board and the bus I2C communication between devices are present.

Following there are the schematic sheets, starting from the FPGA divided for IO banks and presenting in succession the power part, the connectors of the Octopus boards for the signals from the PMTs, the oscillators with all the necessary hardware for the White Rabbit compatibility. In the remaining pages there are the optical transceiver for communication over fiber, the hardware required for configuring the board, embedded instrumentation, connectors, LEDs, buttons for testing and debugging and the FMC expansion connector.

The detailed schematics of the CLB design are in (5).

## 4     CLB LAYOUT

The layout of the Central Logic Board has been designed using the software Allegro PCB Design Editor. The PCB is an object of 12 layers in FR4 material with 317 components (32 integrated circuits), with a thickness of 2.41 mm.

The 12 layers are divided as follows:

- 5 layers for signal routing, TOP, SIG_1, SIG_2, SIG_3, BOTTOM
- 5 layers for ground, GND_1, GND_2, GND_3, GND_4, GND_5
- 2 layers for different power supply, ALIM_1, ALIM_2.

Figure 2 shows the picture of the PCB with the assembled components, and in Figure 3 we see the image of the layer SIG_3 that is one of the inner layers (not visible) where you can note the complexity of routing.



**FIG. 3:** Inner layer (SIG_3) of the PCB.

In the CLB all signals have a differential impedance of 100 ohm. The strictest design rules of the board are: width = 4 mils and minimum spacing = 3.5 mils (under FMC Connector and FPGA areas). The cross section of the board is shown in figure 4.

Special attention was taken for differential pair difference length between p/n:
- SFP Tx & Rx: < 1 mils
- CLOCK signals: < 1 mils
- PMT signals: < 10 mils
- FMC connections: < 5 mils

Special care was taken for differential pair delays inside the following groups:
- PLL CLOCKS: < 10 ps
- Octopus Large & Small: < 100 ps
- FMC CLOCKs: < 20 ps
- FMC Signals: < 300 ps

| | Subclass Name | Type | Thickness (MIL) | Dielectric Constant | Loss Tangent | Shield | Width (MIL) | Impedance (ohm) | Coupling Type | Spacing (MIL) | DiffZ0 (ohm) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | SURFACE | | 1 | 0 | | | | | | |
| 2 | TOP | CONDUCTOR | 1.4 | 1 | 0 | | 5 | 59.406 | EDGE | 5 | 100.39 |
| 3 | | DIELECTRIC | 4 | 4.3 | 0.035 | | | | | | |
| 4 | GND_1 | PLANE | 1.4 | 1 | 0 | ☒ | | | | | |
| 5 | | DIELECTRIC | 8 | 4.3 | 0.035 | | | | | | |
| 6 | SIG_1 | CONDUCTOR | 0.7 | 1 | 0 | | 4 | 63.028 | EDGE | 4 | 98.217 |
| 7 | | DIELECTRIC | 8 | 4.3 | 0.035 | | | | | | |
| 8 | GND_2 | PLANE | 1.4 | 4.5 | 0.035 | ☒ | | | | | |
| 9 | | DIELECTRIC | 8 | 4.5 | 0.035 | | | | | | |
| 10 | SIG_2 | CONDUCTOR | 0.7 | 4.5 | 0 | | 4 | 60.278 | EDGE | 6 | 101.09 |
| 11 | | DIELECTRIC | 8 | 4.5 | 0.035 | | | | | | |
| 12 | GND_3 | PLANE | 1.4 | 1 | 0 | ☒ | | | | | |
| 13 | | DIELECTRIC | 8 | 4.3 | 0.035 | | | | | | |
| 14 | ALIM_1 | PLANE | 1.4 | 1 | 0 | ☒ | | | | | |
| 15 | | DIELECTRIC | 8 | 4.3 | 0.035 | | | | | | |
| 16 | ALIM_2 | PLANE | 1.4 | 1 | 0 | ☒ | | | | | |
| 17 | | DIELECTRIC | 8 | 4.3 | 0.035 | | | | | | |
| 18 | GND_4 | PLANE | 1.4 | 1 | 0 | ☒ | | | | | |
| 19 | | DIELECTRIC | 8 | 4.3 | 0.035 | | | | | | |
| 20 | SIG_3 | CONDUCTOR | 0.7 | 1 | 0 | | 5 | 57.411 | EDGE | 6 | 98.646 |
| 21 | | DIELECTRIC | 8 | 4.3 | 0.035 | | | | | | |
| 22 | GND_5 | PLANE | 1.4 | 1 | 0 | ☒ | | | | | |
| 23 | | DIELECTRIC | 4 | 4.3 | 0.035 | | | | | | |
| 24 | BOTTOM | CONDUCTOR | 1.4 | 1 | 0 | | 5 | 59.406 | EDGE | 5 | 100.39 |

Total Thickness: 94.7 MIL

Layer Type: ALL    Material: ALL    Field to Set: Thickness    Value to Set: [ ]    Update Fields

☑ Show Single Impedance
☑ Show Diff Impedance

OK    Apply    Cancel    Refresh Materials ->    Help

**FIG. 4** CLB Cross section.

In order to respect these rules we adapt the net lengths, as seen in Figure 5.
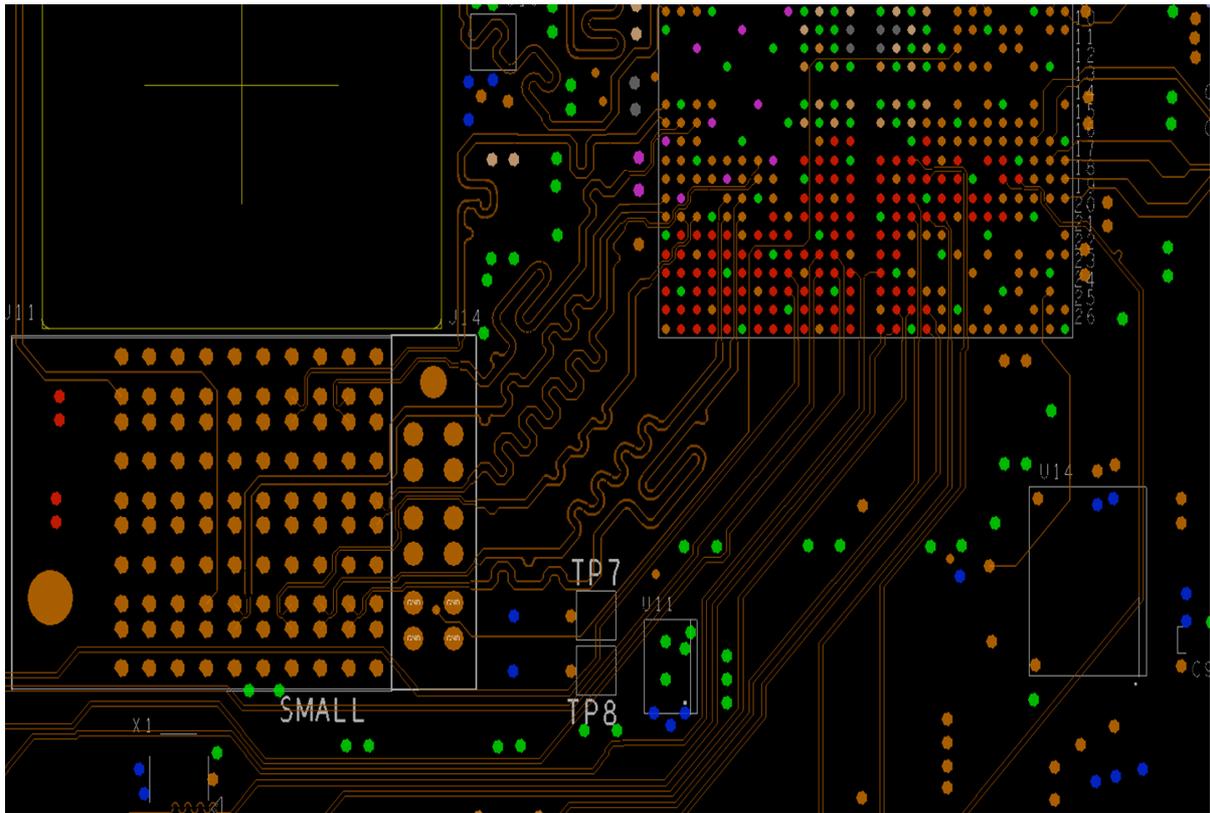
**FIG. 5** Equalized delays on the inner layer SIG_2.

Great attention has been devoted to the power distribution of the board. There are 15 power rails. Two layers were dedicated for routing of these traces. Figure 6 (layer ALIM_1) shows a detail of the hard manually work that has been done for creating and separating the different power planes especially under the FPGA that requires different power supplies.

Different colors means different nets.

## 5 PROTOTYPYNG, TESTING AND PRODUCTION

Several prototype runs have been made: the first 8 boards were produced in Italy and Spain to compare the production quality. In both cases the boards performed well and all the specifications were met.

Test bench were setup in four sites: Genova, Valencia, Amsterdam and Bologna. Extensive debug have been carried out (4) and the 4 setups have been used to speed up the firmware/software development. The design has been validated and no major issues blocked the project. A second prototype run was needed to solve small issues, like connector and fixing holes positioning.

Then a preserie of 20 pieces have been assembled and used to start the integration of the first DOMs.
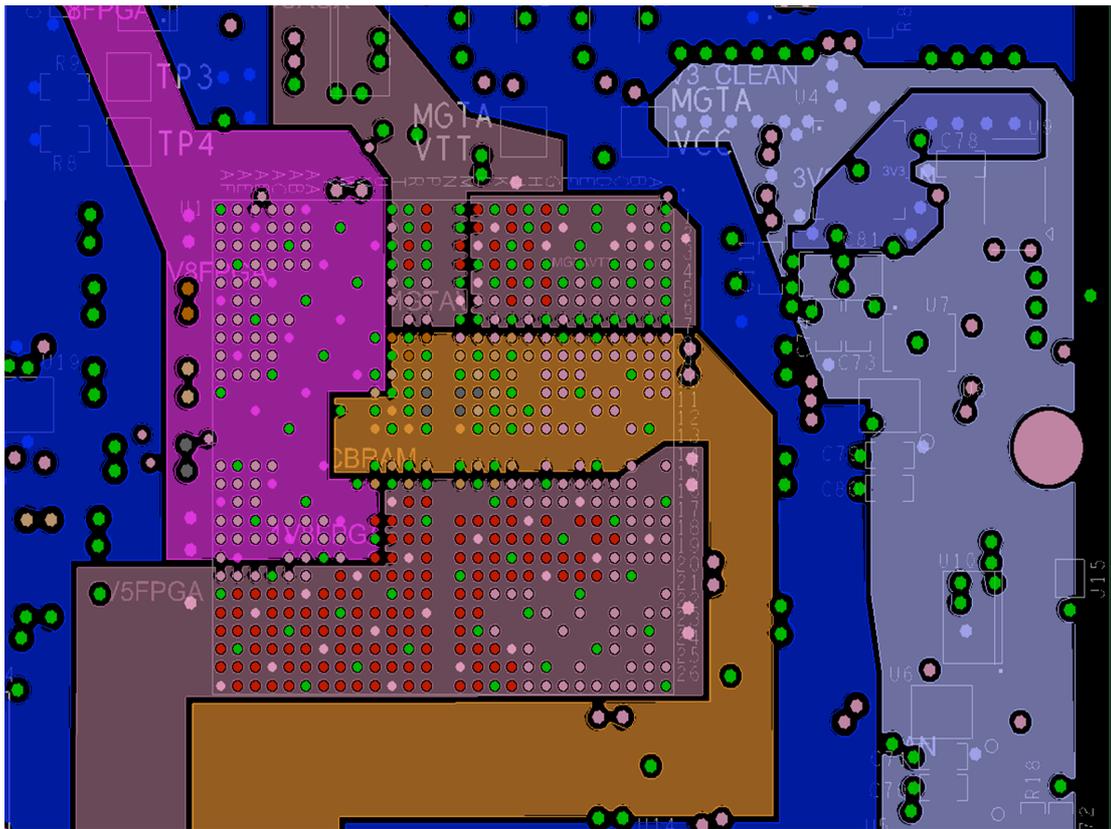
**FIG. 6** Areas of different power supply (ALIM_1).

The production of all the needed CLBs (600 pieces) have been assigned and all the pieces have been built by end of November 2014.

The entire CLB project flow started at the beginning of May 2013 and in 18 months we finished the production of a quite complicated board. All the CLB will pass a burn-in test before sending them to the integration sites, to guarantee that only good boards will be used in the DOMs.

# 6   REFERENCES

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