ISTITUTO NAZIONALE DI FISICA NUCLEARE
Sezione di Genova

INFN-13-12/GE
3rd July 2013

Digital Hydrophone Signal Acquisition and Analysis for KM3NET

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Abstract

The KM3NeT project foresees the utilization of hydrophones for various purposes such as positioning calibration, oceanographic measurements and possibly neutrino detection. Hydrophones will be connected to the Control Logic Board (CLB) inside Optical Modules, were incoming data will be acquired, packed and sent to the On-Shore station.

It is planned to use hydrophones with a digital output, encoded with the AES3 protocol with a sample rate of 192 kHz and an amplitude resolution of the signal of 24 bits. This output is directly provided by the digital hydrophone, or by a digitizer in case of an analog one. The present document will report the result of the interfacing of a digital hydrophone to the Kintex 7 FPGA describing hardware and firmware; in case of the utilization of an analog hydrophone for the final design, there will probably be modifications in the hardware, while the firmware part can be the same in both cases.

PACS:07.50.-e

Published by **SIDS-Pubblicazioni**
Laboratori Nazionali di Frascati

1 General overview

The digital hydrophone HS-DH ([1]), used for note, has the features reported in tab. 1.

Specification	Unit	Value
Receiving sensitivity high gain	dB re 1V/μPa @ 1 kHz	-150
Receiving sensitivity low gain	dB re 1V/μPa @ 1 kHz	-180
Linear frequency range	Hz (3 dB variability)	5-80,000
Beampattern - Horizontal Plane	($\pm$ 1.5 dB)	Omni upto 80 kHz
Beampattern - Vertical Plane	($\pm$ 2.0 dB)	within 240° upto 80 kHz
Equivalent input noise (High gain)	dB re μPa/$\sqrt{\text{Hz}}$ @ 10 kHz dB re μPa/$\sqrt{\text{Hz}}$ @ 1 kHz	+33 +37
AD converter		2 ch 24 bit $\Sigma\Delta$
Sampling frequency	kHz	192
Dynamic range	dB	110
Digital full scale	V ptp @ 10 kHz	6
Digital output protocol		AES/EBU
Power supply: voltage	V_{DC} (reversed polarity protection)	5 to 18
Power supply: current	mA (12 V)	65
Max operation depth	m	1000
External coat		Polyurethane and marine stainless steel

Table 1: AGUAtech digital hydrophone features

The incoming signal has to be adapted in order to interface with the FPGA, converting the signal from 5 V to 2.5 V. In the concept of the CLB, The incoming data has to be decoded and stored in a local FIFO, from where they will be read and packed with all the other data to be sent On-Shore.

In order to test the correctness of incoming data, the Xilinx KC705 Development Board was used; the interface board has been plugged in using the J46 connector, and

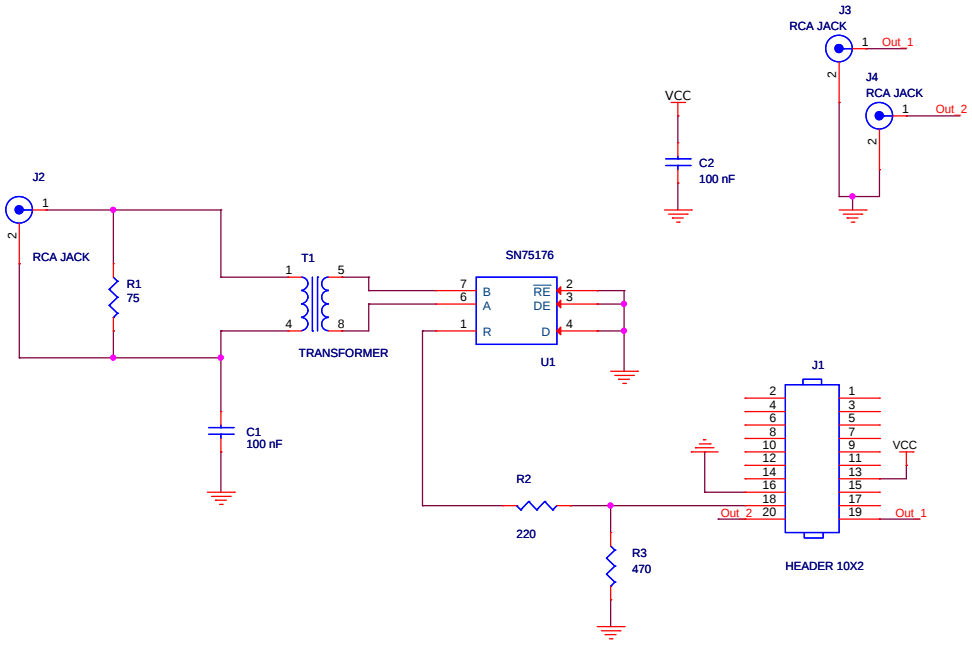

Figure 1: Hydrophone interface board schematic.

additional resources available on the KC705 board were used.

The sample rate of 192 kHz of the hydrophone, with words of 64 bits (two 24 bits audio channel and 16 bits of info), produces an incoming rate of 12.288 Mbps, which is much higher than the fast speed of 921,600 bps of the UART, making necessary a temporary storage of data inside the FPGA.

The basic idea of the test measurement is the following: record the incoming data for a period of some tens of seconds, then download the data to a PC using the UART to analyze it offline.

2 Hardware design

The signal outcoming from the hydrophone needs to be adapted in order to be read by the FPGA. A simple board was made as shown in fig. 1, to meet the LVCMOS25 standard.

The board provide also two output connectors, to have an easy way of connecting oscilloscope probes. These outputs have been used for preliminary tests to compare the incoming signal from the hydrophone and a mirrored signal outcoming from the FPGA, in order to be sure of the correctness of signal levels.

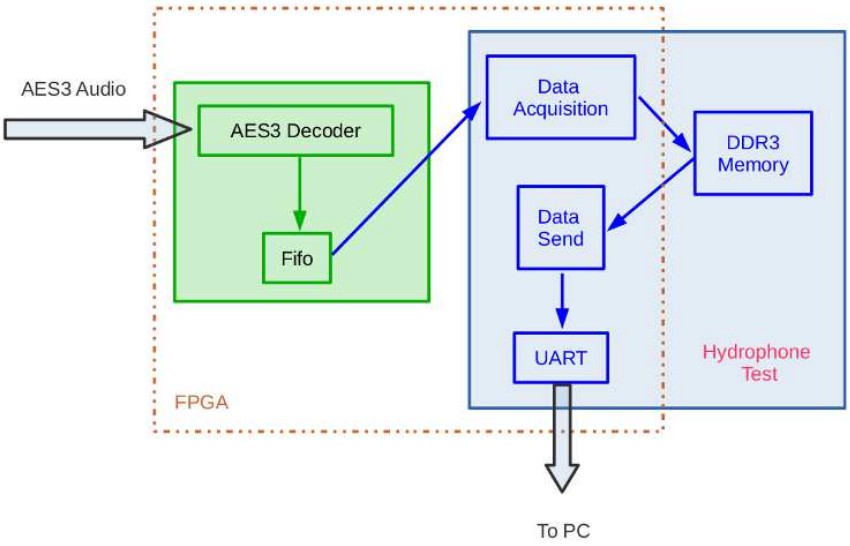

Figure 2: Block scheme of the firmware design: components for the final CLB design (green), components added for the test (blue).

3 Firmware design

The firmware design has been subdivided in two parts, in order to have a section dedicated to the decoding of the incoming AES3 audio input from the hydrophone, which will be inserted in the final design, and an other dedicated to the test measurements (see fig. 2).

3.1 AES3 Decoding module

The used AES3 decoding module is provided by Xilinx (*https://secure.xilinx.com/webreg/clickthrough.do?cid=119758*) and full documentation can be found in [2]. As shown in fig. 3, the receiver module is subdivided in three different parts:

AES3 DRU: over-samples the incoming audio bitstream, detecting the length of a state (half a bit, AES3 protocol uses a Biphase-Mark Encoding), and picks a sample point approximately in the center of the state to sample each states value.

AES3 Framer: detects the preamble sequences so that the data can be aligned properly to the sub-frame boundaries. The framer decodes the Biphase-Mark symbols and then deserializes the data into 8-bits bytes properly aligned so that each sub-frame is output from the framer in four consecutive bytes.

AES3 Formatter: takes the data from the framer and formats it into audio sample words and valid, channel status, and user data bits for each of the two audio channels. It also detects parity errors.

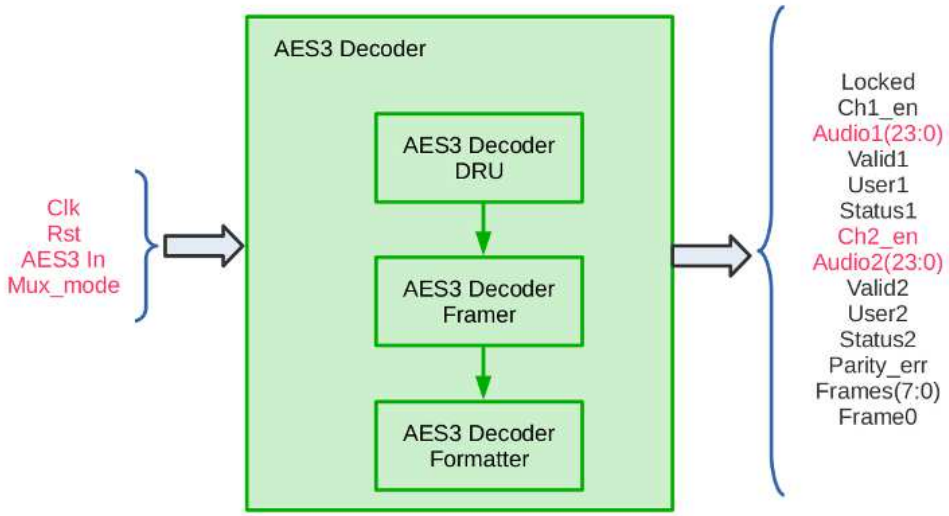

Figure 3: Block scheme of AES3 receiver module.

The clock provided to the module must be at least four times the bitrate of the incoming audio signal, in order to allow the *AES3 DRU* module to properly sample the data. Using a 192 kHz audio signal, the AES3 protocol has a bit rate of 24.576 MHz; for this reason a 100 MHz clock or faster should be used.

Notes

A bug was found in the *AES3 DRU* module, which cause the wrong sample of the incoming bitstream. The involved code is listed below:

```
[samepage=true]
process(clk)
begin
    if rising_edge(clk) then
        if edge_detect = '1' and update_min = '1' then
            -- bug: add 1 to the counter
            min_hold <= min_capture + 1;
        end if;
    end if;
end process;
```

this part of code is used to detect the length of a state (half a bit) of the incoming audio bitstream; the `min_capture` signal contains the minimum value of clock steps between two edges of the bitstream, which is periodically updated in order to detect a

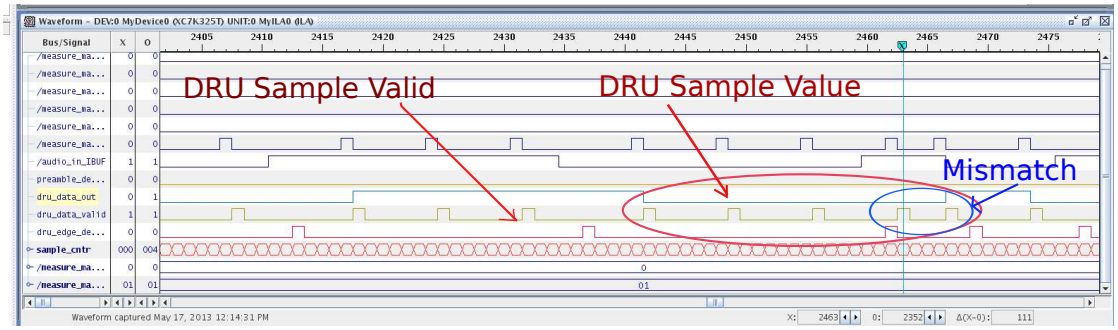

Figure 4: Example of mismatch caused by the bug: the wrong sampling time (which is one clock shorter) originates an additional sample, which doesn't allow the detection of the preamble of the new AES3 sub-frame.

possible change in the bitrate. This value is stored in the `min_hold` signal, used for the sampling: an additional counter (`sample_cntr`) is always increasing each clock, and is reset when a new edge of the bitstream occurs or the `min_hold` value is reached; a new value (half bit) is sampled at `min_hold / 2`.
A `+ 1` has to be added when assigning `min_hold`*, in order to achieve the right sample time, otherwise the correctness of bit values will be compromised, particularly in the preamble detection, in which bitstream edges are far each other (see fig. 4).*

3.2 Test modules

To test the decoding of the hydrophone signal, a separate section has been added to the firmware. Tests are made in 3 steps:

1. Data acquisition
2. Data sending to PC
3. Data analysis

Data acquisition is achieved by the switch button SW2 of the KC705; during this phase, the decoded data from the AES3 Decoding module are read from the FIFO and written in the DDR3 SDRAM memory of the KC705. In this way it is possible to fully record a measurement of the desired duration (even minutes).

Data transfer to a PC using the UART at 921,600 bps is possible by pressing the switch button SW4 of the KC705, once a measurement is finished.

Data are received by a PC and saved in binary files, ready for the post analysis.

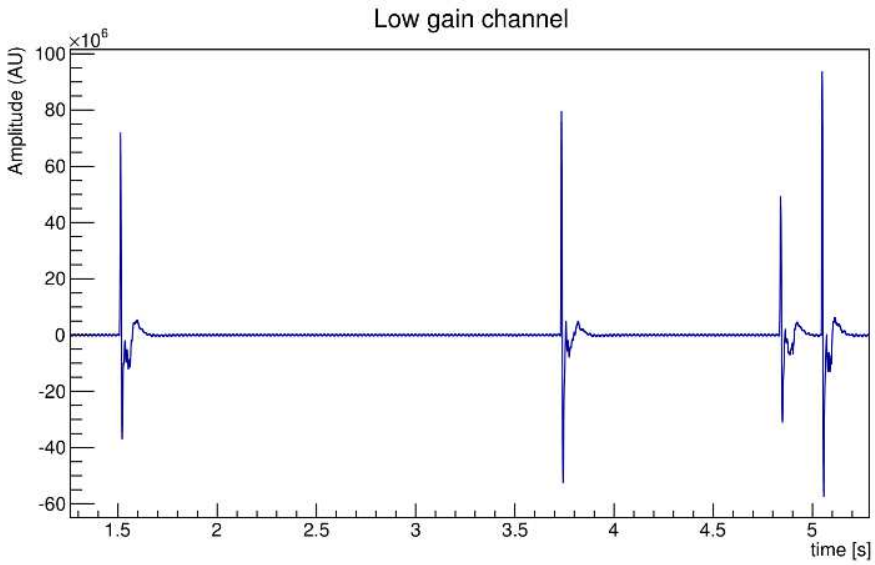

Figure 5: Acquired data from the hydrophone in air at 192 kHz of sampling rate; the stimulus, caused by hitting the hydrophone with a finger, are clearly visible.

Fig. 5 shows the audio signal of the low gain channel of the hydrophone in air, while in fig. 6 are shown the additional 16 bits of info present in each frame decoded by the *AES3 Decoding module*. The AES3 protocol subdivide data in sub-frames, in which there are a preamble, 24 bits with the signal amplitude and four additional bits (validity, user, status and parity error). Two sub-frames make a frame, containing the sampled signal in two channels (in our case the first channel is a high gain, while the second is a low gain). User and status bits (for both channels) contained in each frame, should be packed to form a 192 bits word; to do that it is present an 8 bits counter, named *frame number*, which can be used to perform the right alignment of the words. As it is possible to see, the frame number is continuously increasing, showing that there are not loss of packets. In addition it is possible to see that the flags, containing the frame0, validity, user, status and parity error bits have always the same value except when the *frame number* is equal to 0, because in that case the *frame0* bit value is one (this signal can be used to build the 192 bits words, too). The meaning of this is that the additional info are not used in the hydrophone and no parity errors occurred.

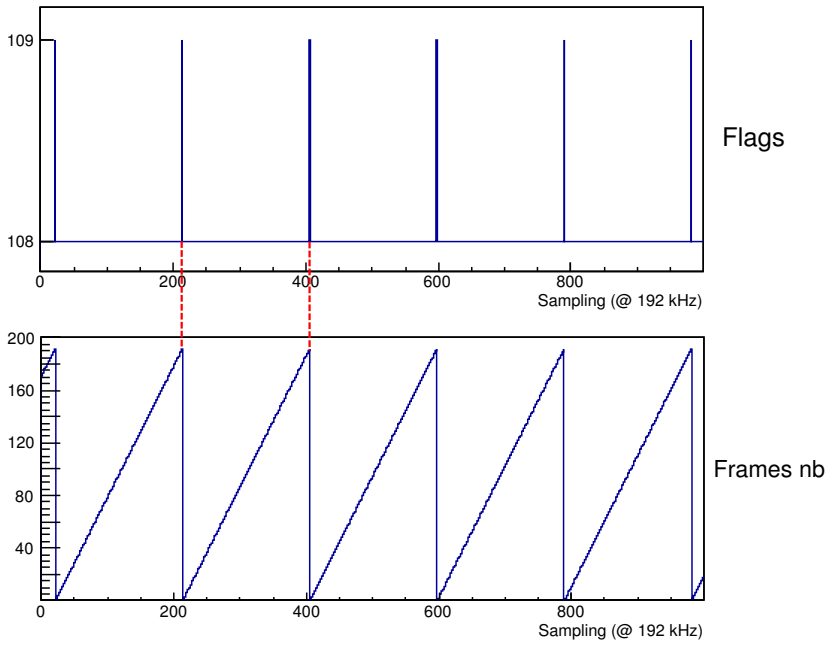

Figure 6: Flags bits (top) of each sampled frame and Frame number (bottom).

4.2 Water measurement

Fig. 7 shows a scheme of the instrumental apparatus we used for water measurements. The hydrophone was awash in a bucket with water, and a wooden plate was used to transmit the sound emiited by a speaker to the bucket. A plastic foam was used to reduce floor vibrations.

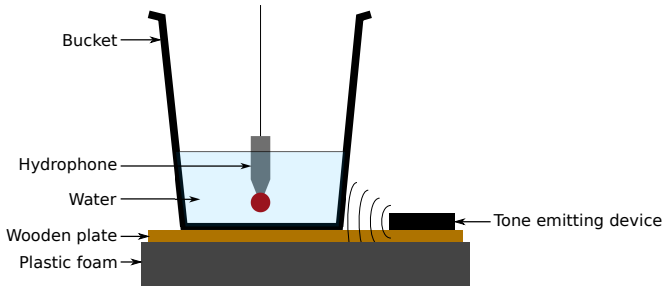

Figure 7: Instrumental apparatus for water measurement.

In fig. 8 is shown the FFT of the audio signal when the hydrophone was stimulated with sounds at 440 Hz (A tone) and 330 Hz (E tone). In the same graph it is possible to see also some noise at 350 Hz, multiple of the 50 Hz noise.

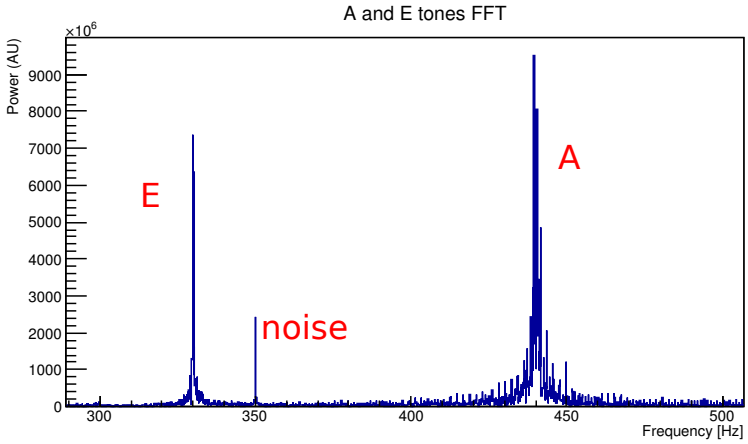

Figure 8: FFT of audio signal with stimulus at 330 Hz and 440 Hz; noise at 350 Hz is also visible (multiple of the 50 Hz).

References

[1] *http://www.agua-tech.com*

[2] Xilinx, *XApp1014[V1.2]*, November 9, 2009.