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Trigger Handling and Distribution in the KLOE Experiment

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Abstract

This document describes the architecture of the KLOE Trigger handling and distribution system. It is based on 4 types of VME modules specifically designed for the KLOE experiment: the Trigger Supervisor, the Fan In/Out board, the Trigger Distributor and the Trigger Receiver.

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1. Introduction

Although the general overview of the Data Acquisition and Trigger Systems was already given elsewhere,[1,2] we now recall the essential information and define some terms that will be used in the text.
A two level concentration has been chosen in KLOE for the Read-out System:

- the first level (L1), performs data concentration at the VME crate level, using a custom bus (AUXbus) and a dedicated Read-Out Controller (ROCK); [3]
- the second level (L2), concentrates the data coming from a group of VME crates, via a custom cable bus (Cbus) towards a Read-Out Controller Manager (ROCKM) which, in turn, is read-out via standard VME bus by a Processor that prepares the data in a string of sub-events and sends them to the On-line Farm via a FDDI interface.

The KLOE trigger system has been designed to work at two different levels[1]:

- the first level trigger (T1), which uses data from the electromagnetic calorimeter and drift chamber multiplicity, and is ready in less than 200 ns, at a rate of about 20 KHz (at the full Daphne luminosity);
- the second level trigger (T2), which is produced after about 1.5 - 1.8 μs, to validate the first level trigger, with a rate not exceeding 10 KHz[2].

Only the T2 signal is required for ROCKs, ROCKMs and the Drift Chamber TDCs, while T1 and T2 are both required for calorimeter's ADCs and TDCs. Moreover, in order to be a good reference time, T1 must be generated with a maximum jitter of the order of 50 ps for the calorimeter TDCs while the Drift Chamber TDCs can accept 1 ns jitter on T2. Different hardware solutions have then been chosen for the first and second level trigger distribution and are described in what follows.
Due to the high frequency of the two levels of trigger, the KLOE collaboration decided to avoid the distribution of the trigger number to the Front-End Electronics (ADC & TDC modules). At every T2 signal a local trigger number is incremented in all the ADCs, TDCs, ROCKs and ROCKMs modules and the content of the ADCs and TDCs digital data is stored into the local buffers.
The Trigger Number in each Front-end board and in the ROCKs is a 12-bit counter (that overflows every 4096 triggers and starts again from zero). A unique 32 bits Run Trigger Number (RTN) is generated inside the TORTA and the Trigger Supervisor. The first one is read-out together with the Trigger information on every event, the second one is used by the Data Flow Control (DFC) processor during the data taking to schedule the event flow to the On-line Farm. This complements the Event Number that is generated and imposed at the level 2, before the event building stage.

To check that the synchronization of all the independent Trigger counters is not lost with time, a cyclic test against a reference trigger number (Golden Number) is performed. The Golden Number is a global 12-bit parameter defined at the start of run and the mechanism used to find possible mismatches is described in chapter 6.

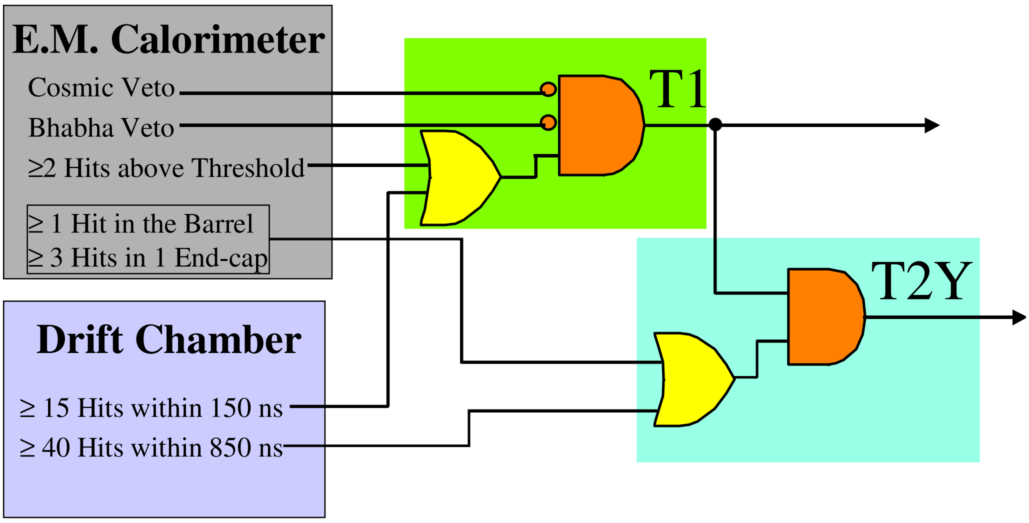

Fig. 1 – Block diagram of the two levels Trigger

2. Trigger Signals

Some definitions of the trigger signals and protocols are given:

- T_0 is the time at which the real event occurs.
- T1 is the first level Trigger that has to be ready within 200 ns after T_0. It is generated by the Trigger final decision board (TORTA), using the information coming from the Electro-Magnetic Calorimeter (E.M.C.), and from the early arriving hits in the Drift Chamber (D.C.)[1] synchronized with the accelerator frequency, and then distributed by the Trigger Distributor (TD) (Fig.1 & 2).
- T2Y is a signal, generated by the TORTA as a second level trigger, which takes into account the information from the Drift Chamber. It is ready and sent to the Trigger Supervisor (TS) at a time between 200-1500 ns after T1 (depending if it is an E. M. C. validated trigger or a D. C. trigger).
- T2 is generated by the TS with a constant delay of about 1.8 – 2 µs after T1 and distributed if a T2Y from the TORTA was received. Its jitter needs to be better than 1ns because the Chamber TDCs will use it as a reference time.
- T1ACK is an acknowledge level which is asserted by the TS upon the receipt of a T1 signal from the TORTA. It is de-asserted at the end of the fixed time delay, independently of an eventual T2 generation, and if no BUSY condition is detected by the TS. T1ACK acts as a DISABLE signal to the TORTA. In case of a Golden Number Trigger, T1ACK remains asserted during the synchronization cycle.

- A BUSY condition in an ADC/TDC L1 crate means that, at least one of the Front-End Electronics buffers has space for only one more event (that could be generated before the BUSY condition is detected by the TS).
- HALT is the signal raised by the ROCK(M) in case of error.
- TBERR is an error line, asserted by the TORTA, if a T1 signal is not followed by a T1ACK from the TS or if internal errors are detected.
- TSLATCH is an error line on the backplane of the TS crate. It is asserted in case of errors revealed by the TS and causes the freezing of the status of all the lines in the Fan-In/Out (FIO) modules in dedicated VME registers with single bits, representing the status of each line (incoming or outgoing).
- SYNCREQ is a signal activated by the TS, in case of a Golden Number check cycle, and distributed by the FIOs to all the ROCKs and ROCKMs.
- SYNCFAIL signal is the answer of all the ROCKs and ROCKMs to SYNCREQ and is received by the FIOs. When all these signals are released the check is successfully completed.

A more detailed description of the usage of all these signals follows in the next chapters.
The relative timing of the all the relevant signals in case of a normal trigger cycle and of a synchronization cycle are shown in Fig.4 and 5 respectively.
The trigger signals already described are consistent with a fixed dead time in KLOE of around 2μs/Trigger (T1) which in turn means that with a First Level Trigger rate of 20 KHz, the Dead Time is around 4%.

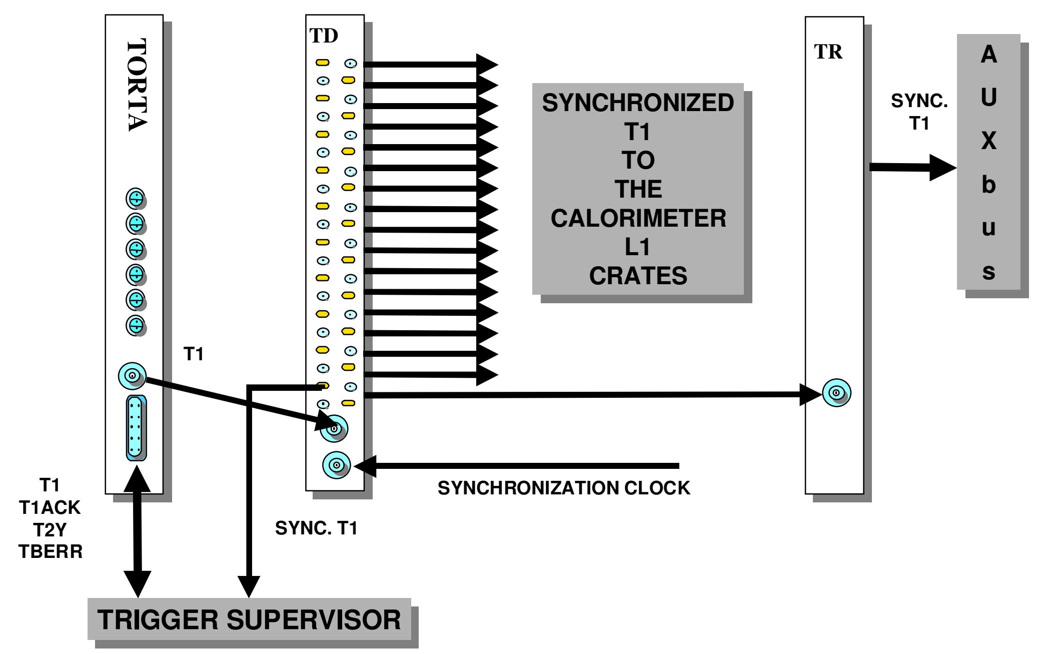

Fig.2 – Trigger Distribution

3. The Trigger Distributor and Trigger Receiver

One of the most critical signals is T1, which is distributed to the ADCs and TDCs via the AUXbus backplane by using one of the available spare lines.
Obviously 1ns of time precision is already an issue, but 50 ps require a more sophisticated and cautious design of the line.
The Trigger Distributor (TD)[5] distributes the T1, directly received from the TORTA, synchronizing it at 92.06 MHz, 1/4 of the DAΦNE machine clock (368.25 MHz). The synchronized T1 is then fan-out, via a dedicated coaxial cable, to the Trigger Receivers (TR), 9U VME modules, housed in the 17th AUXbus slot of each L1 crate of the E.M. Calorimeter. The TR then distributes it, to the modules in the crate, via AUXbus backplane (Fig.2).

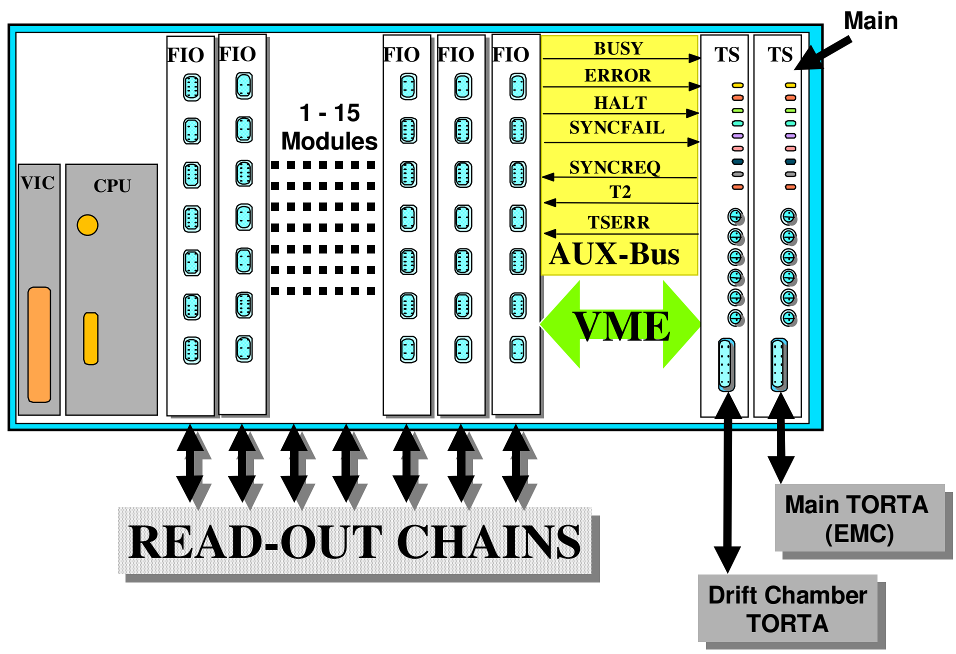

Fig. 3 – Trigger Supervisor Crate

4. The Trigger Supervisor and FIO System

The trigger supervisor (TS)[4] is a 9U VME board in a crate (Fig.3) with an AUXbus backplane. In the same VME crate there are at least 12 Fan In-Out (FIO)[5] modules, one for each readout chain (we actually foresee 12 chains in the DAQ), that distribute the trigger signals to the ROCK and the ROCKM in any L1 crate in the chain.
Every FIO module receives the T2 and SYNCREQ signals from the TS via backplane, and redirects the OR of the BUSY and SYNCFAIL signals, coming from the ROCK(M)s to the TS, using dedicated AUXbus backplane lines.
Two other signals are also used on the backplane in the handshaking between TS and FIOs:

- FIOSyncAck: asserted by the FIO to acknowledge the receipt of the SYNCREQ signal.

- FIOSyncOK: asserted by the FIO when all the chain ROCKs have correctly replied to the SYNCREQ signal by raising SYNCFAIL.

Both signals are Wired-Or lines, but the FIOSyncAck is normally LOW and is active HIGH, while FIOSyncOK is normally HIGH, becomes LOW on SYNCREQ and then returns HIGH on successful completion of the cycle.

5. Normal Running

The T1 signal is received by the Trigger Receiver, via a dedicated front-panel coaxial connector, and then asserts the T1 signal on the AUXbus.

The ROCK(M) has a 5 line NIM multi-coaxial connector on the front-panel; it receives the T2 signal on one of these lines and implements the function of trigger assertion (T2) on the AUXbus. The rest of the front-panel connector lines are dedicated to SYNCREQ (from the FIO), SYNCFAIL, HALT and BUSY (from the ROCK).

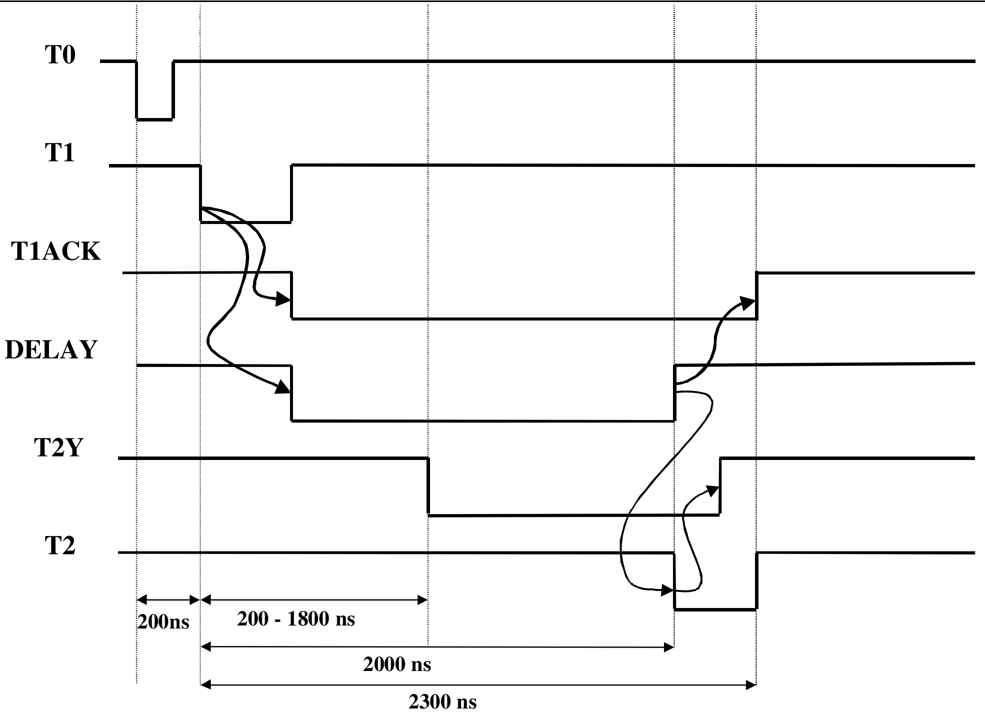

Fig. 4 – Trigger Timing during Normal DAQ cycles

6. Trigger Synchronization Cycle

The synchronization test cycle is required to check that the trigger numbers, independently generated by ROCKs, ROCKMs and ADC/TDC boards, continue to be aligned during the run. The Trigger system is in charge of requiring the execution of this cycle every time (or only some time) the last generated trigger number is exactly a Golden Number.

The cycle is activated in all the ROCKs and ROCKMs when the Trigger Supervisor and the FIO system assert the SYNCREQ signal and the previous readout cycle is completed. The correlated signal, SYNCFAIL, is asserted by the ROCK(M) at the end

of the synchronization cycle if no error is detected. The BUSY signal is asserted by the ROCK(M)s when the cycle starts and released at the end, if successful.
During this SYNCREQ cycle, the ROCK tests that the last generated trigger number is equal to the Golden Number memorized at the run configuration time. If no internal error (after a check of it's own trigger counter) is detected, the ROCK checks the last generated trigger number from every ADC/TDC. In case of mismatch, the address of the slave with the wrong trigger number is written in a dedicated register in the ROCK then a HALT signal is asserted at the completion of the cycle, while the BUSY signal remains asserted until a general reset is generated. SYNCFAIL is not generated in case of mismatch and the Trigger Supervisor uses both a timeout on SYNCFAIL and the assertion of the HALT signal to detect the failure.

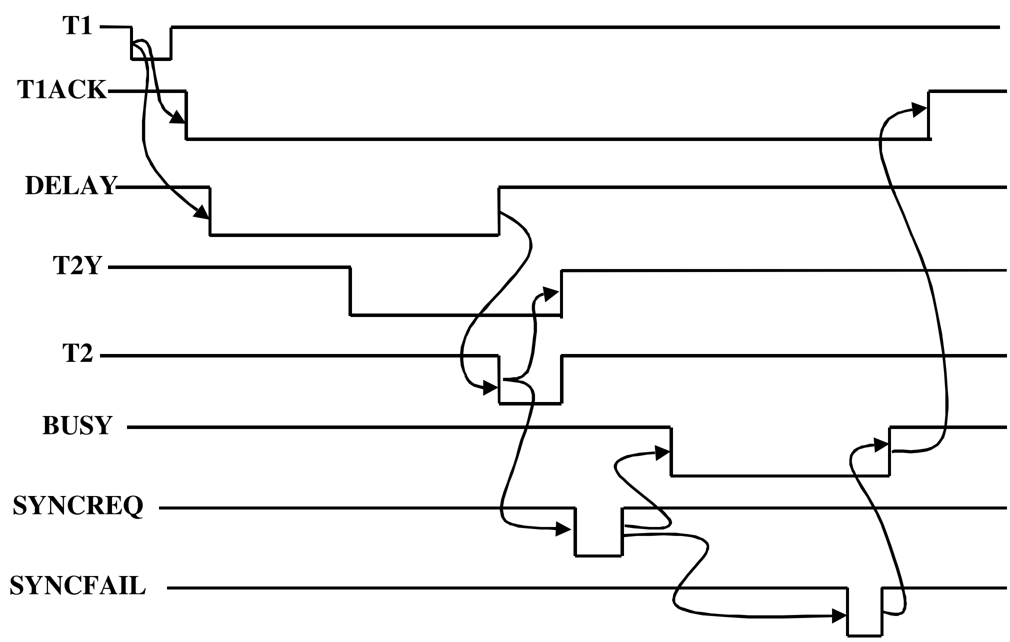

Fig. 5 – Trigger Timing during Synchronization Check Cycle

As already stated, in case of an error condition, a VME operation is required to restart the AUXbus activity. No information is transmitted to the ROCKM in the chain if a failure is discovered by a ROCK. The ROCKM also makes a test of the Golden Number against it's own internal counter and the eventual failure is written in a VME register.
The SYNCREQ cycle can be 10 µs long in a completely configured crate, but the start time in every crate depends on the completion of the remaining read-out operations in the ROCK finite state machine; a synchronization cycle can only be started between two event readouts.

7. Error Handling

After a timeout, a failure in the synchronization check, or in case of a protocol error, the Trigger Supervisor asserts the TSLATCH line on the backplane (see chapter 2 before), stops the Trigger generation by holding the T1ACK signal and sets an error

flag in a VME register. This flag is read-out by the Trigger Supervisor Processor, a VME CPU sitting in the same crate and running the Trigger Control Program, that in turn generates a DAQ Error Message to the DAQ system.
In case of a mismatch, the events already recorded on tape can not be easily eliminated during the off-line production. Retaining those events in memory, until the next synchronization cycle is successfully completed, requires that every CPU registering events on tape writes events corresponding to a given time interval between two synchronization cycles, only when the next cycle is successfully completed.
Dedicated output buffers for at least two time intervals (plus the time required to detect and to distribute the failure message) are required, to assure the usage of the tapes in streaming mode. Let's define:

- "n" the number of tapes (n = 10 or less);
- "m" the Golden Number (12 bits can represent 4 k triggers but the SYNCREQ can be started at given multiple "t" of Golden numbers);
- 5 KB the mean size of a single event.

The required memory buffer for two consecutive synchronization cycles comes out to be 40 MB for t = 1 (2.5 synchronization cycles/s) and 400 MB for t = 10 (1 synchronization cycle every 4 s). If we divide it by 10 (= n) FARM CPUs designated to write events on tape, we obtain a minimum of 4 MB of buffer/CPU. Larger Golden Numbers, using multiples of 4096, will be proportionally memory hungry.
In practice there is no strong reason to do the checks very infrequently because, if we account 20 μs as the mean time to accomplish a sync check, in case of a Golden Number with t = 1 this will introduce only 10^{-3} % of increase of dead time. A Golden Number with t = 1 will instead release the need of memory buffers inside the Event Building Farm; the amount of data lost will also be smaller (20 MB = 4 KEvents).
The events in the buffers of the Farm will be released on the following conditions:

- New 'complete' events are coming in, with a trigger number greater than the Golden Number. This implicitly means that the previous Synchronization check was successful; the events in the buffer will be written on tape.
- An End Of Run (EOR) message is received with no errors reported, meaning that the last Sync check was successful. The remaining events in the buffer are written on tape and an EOR record is appended. The events to be written are only those up to the last successful synchronization cycle, otherwise the Trigger Control Process, receiving the EOR message, will try to round up the events to the next cycle stopping the Trigger Supervisor immediately after that.
- An Error condition or an EOR with an error reported are received. This will cause the flush of the present buffers and no data will be written on tape.

8. Conclusions

A detailed description of the Trigger-DAQ interface system has been presented including the functional specifications of all the relevant electronic modules involved.
The system has been already successfully tested both in the KLOE System Test and in the first DAQ tests with part of the Calorimeter Front-end Electronics in the final configuration. T1 rates (with T2 = T1 and fake read-out) of about 300 KHz were reached without significant problems.

REFERENCES
[1] THE KLOE TRIGGER SYSTEM – ADDENDUM TO THE TECHNICAL PROPOSAL – LNF-96/043 (IR) 3 Settembre 1996
[2] THE KLOE DATA ACQUISITION SYSTEM – ADDENDUM TO THE TECHNICAL PROPOSAL – LNF-95/014 (IR) 29 Marzo 1995
[3] A. Aloisio et al., "Fast Read-out System for KLOE", KLOE Note 88.
[4] V. Bocci, G. De Robertis, F. Ruggieri, "The KLOE Trigger Supervisor", KLOE Memo 125.
[5] Trigger Distributor and Fan In/Out modules memo in preparation.