SIDDHARTA Technical Note IR - 5

Progress report on SDD stability improvement

The present note reports the development done for solving long-term stability problems of prototype SDDs, observed during BTF run [1], as well as important detector properties like linearity and high rate response, measured with higher accuracy after eliminating the instability sources.

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A previous study [1] showed that the output signal from prototype SDD setup presents a long-term instability, initially attributed to temperature variation. The reported measurement was done with the SDDs cooled at about –42 C by a one-stage APD cryostat, without temperature stabilization. Consequently, the temperature was stabilized using a home-built high precision PD controller, which allowed setting the temperature within a range of ±0.07 Celsius for both detector and amplifier hybrid. The temperature behavior of SDD socket after stabilization is shown in the figure below.

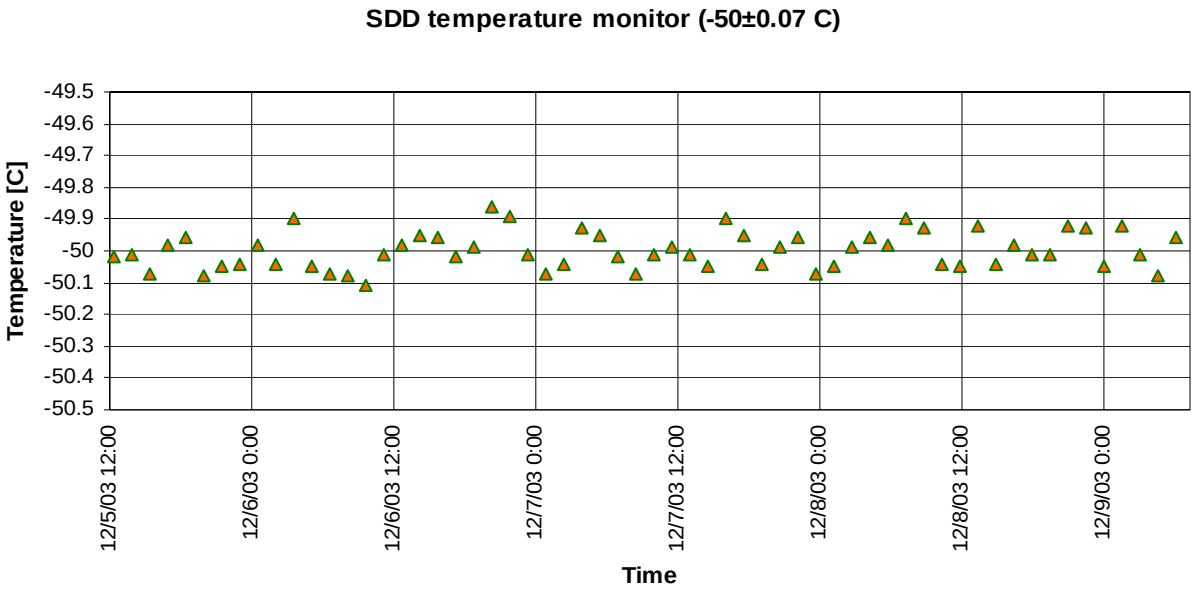

Fig. 1 Temperature stability measurement after installing the controller

As result, no improvement was observed in the SDD gain behavior. Sets of long-term measurements were done at various, stable temperatures. The Mn K_α peak position, measured at successive time intervals for different temperatures, is plotted in Fig 2.

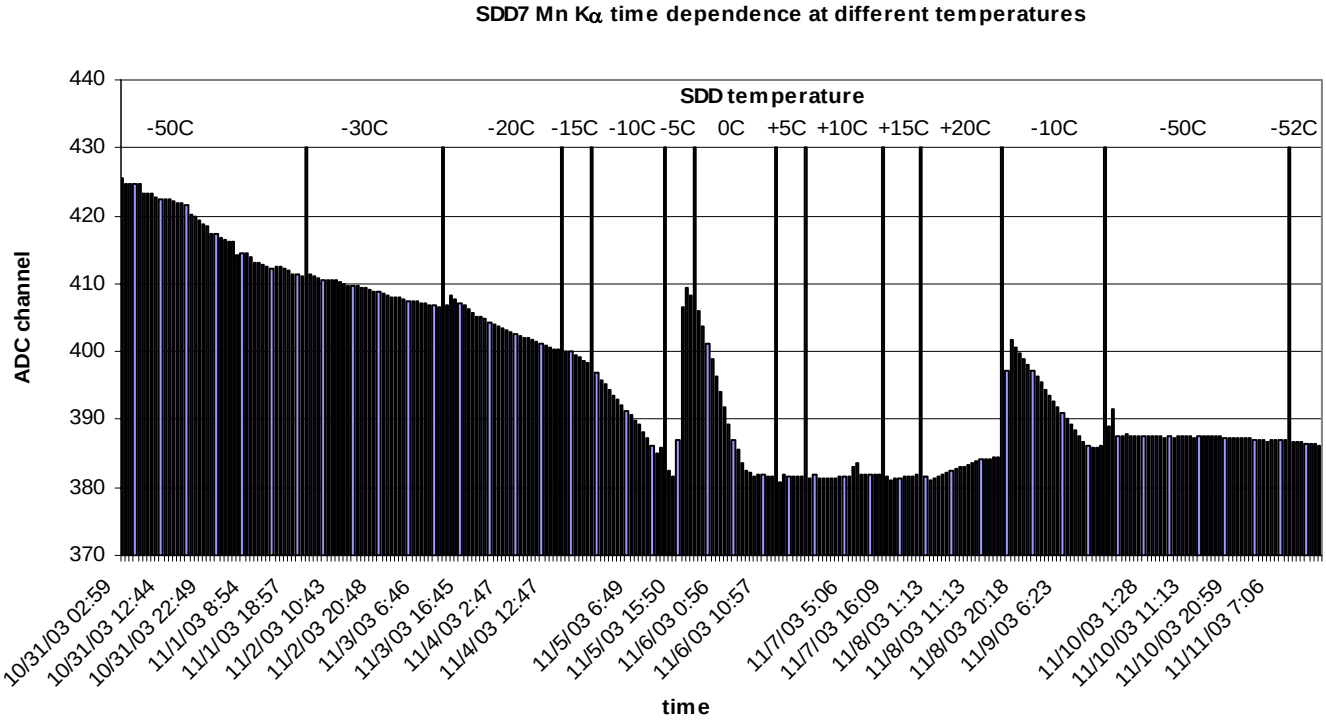

Fig. 2 Mn Kα peak position for sdd7 at various temperatures, over a total period of 15 days

As a general feature, all long-term measurement charts showed a continuous drop of the gain, overlapped by a quasi-periodic fluctuation. Out of the two, the drop was covering a larger range, while the second fluctuation reached at most few channels in amplitude.
This behavior, correlated with the temperature influence (after a long period of operation at room temperature the effect gets smaller -Fig. 2-) indicated that a possible source could be a floating structure which gets charged over time and might influence the output FET capacities. The only structure suspected was the unused reset diode, not bonded.
After bonding the reset diodes on two out of the seven SDDs in the array (4 and 7) and inverse polarizing them by connecting the pins to R1 (–15 V), a new set of measurements was performed.
The result was a major improvement in the gain stability; the dropping trend disappeared on SDDs 4 and 7, which became more stable than non-bonded ones.

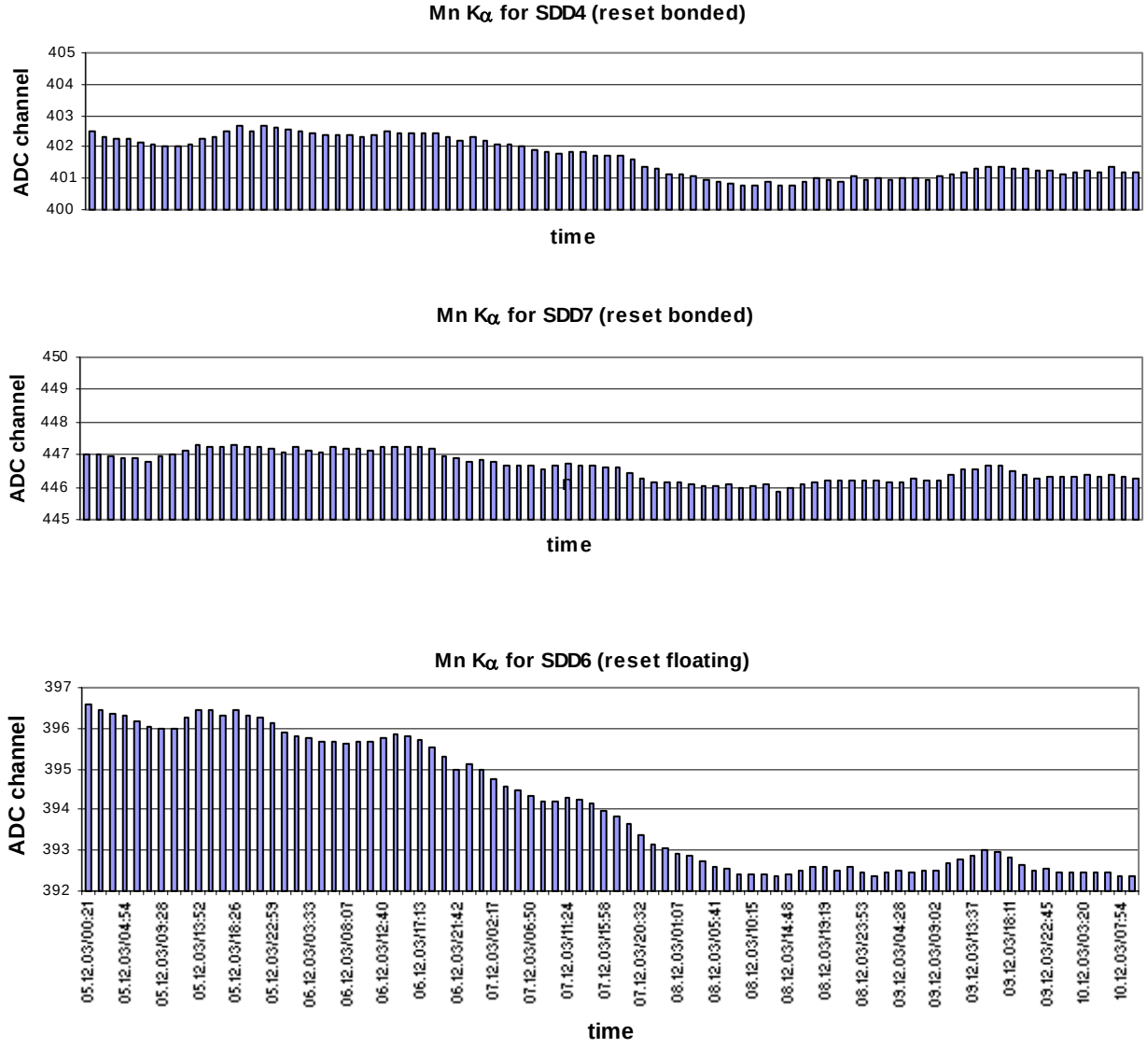

Fig. 3 Bonded reset SDDs (4 and 7) compared with a non-bonded reset one (6)

After having eliminated the major instability source, the remaining problem was the relatively large long-term fluctuation of the Mn Kα (about 20 eV) not correlated with starting up time. The following paragraphs will refer only to SDDs 4 and 7.
Various SDD electrodes which might influence the gain were monitored, by including them in DAQ input array. Out of these, R1 (first drift ring), polarized independently from the rest of rings connected to a voltage divider, was found synchronous with gain fluctuations.

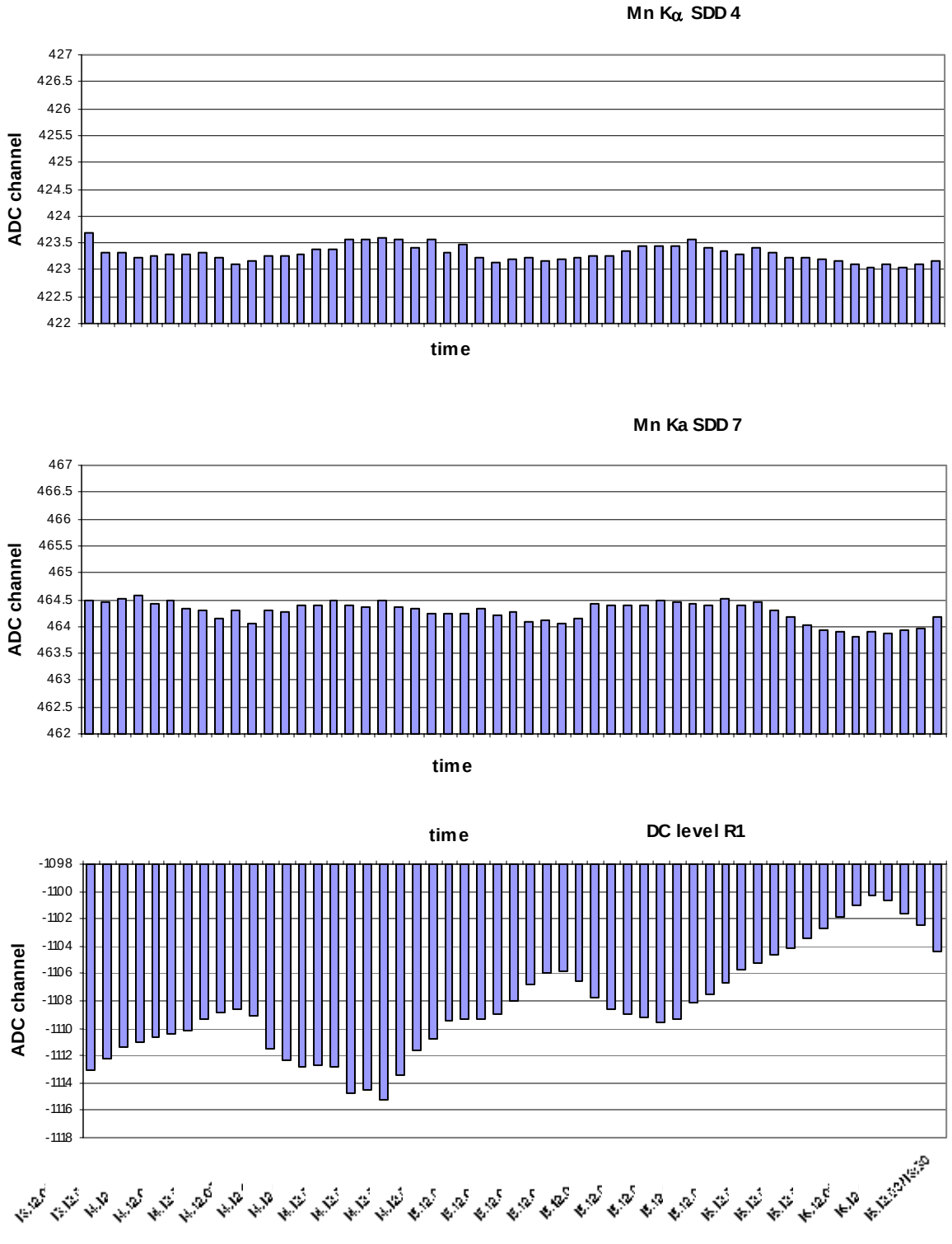

Fig. 4 Mn Kα peak position on SDD 4 and 7 and R1 bias voltage

After the above reported measurement it seemed that R1 voltage was responsible for the gain instability. This voltage is provided by a stabilized supply, and a local filter is mounted on the SDD board to cut-off eventual EM pickup noise from the cables. But R1 sums its bias source current to the one from the last element in the HV chain divider. A test done by varying the HV divider current showed that R1 voltage is strongly influenced by this last one, due to the fact that the local filter vas not calculated to account for this additional current source. Since the HV chain is composed by many FETs and represents a potential source of instability, the R1 filter was redesigned in order to ensure the requested stability. The result was a more stable R1 voltage, but the same level of fluctuation in gain was measured on SDD 4 and 7. In addition, the correlation with R1 voltage was inverted.

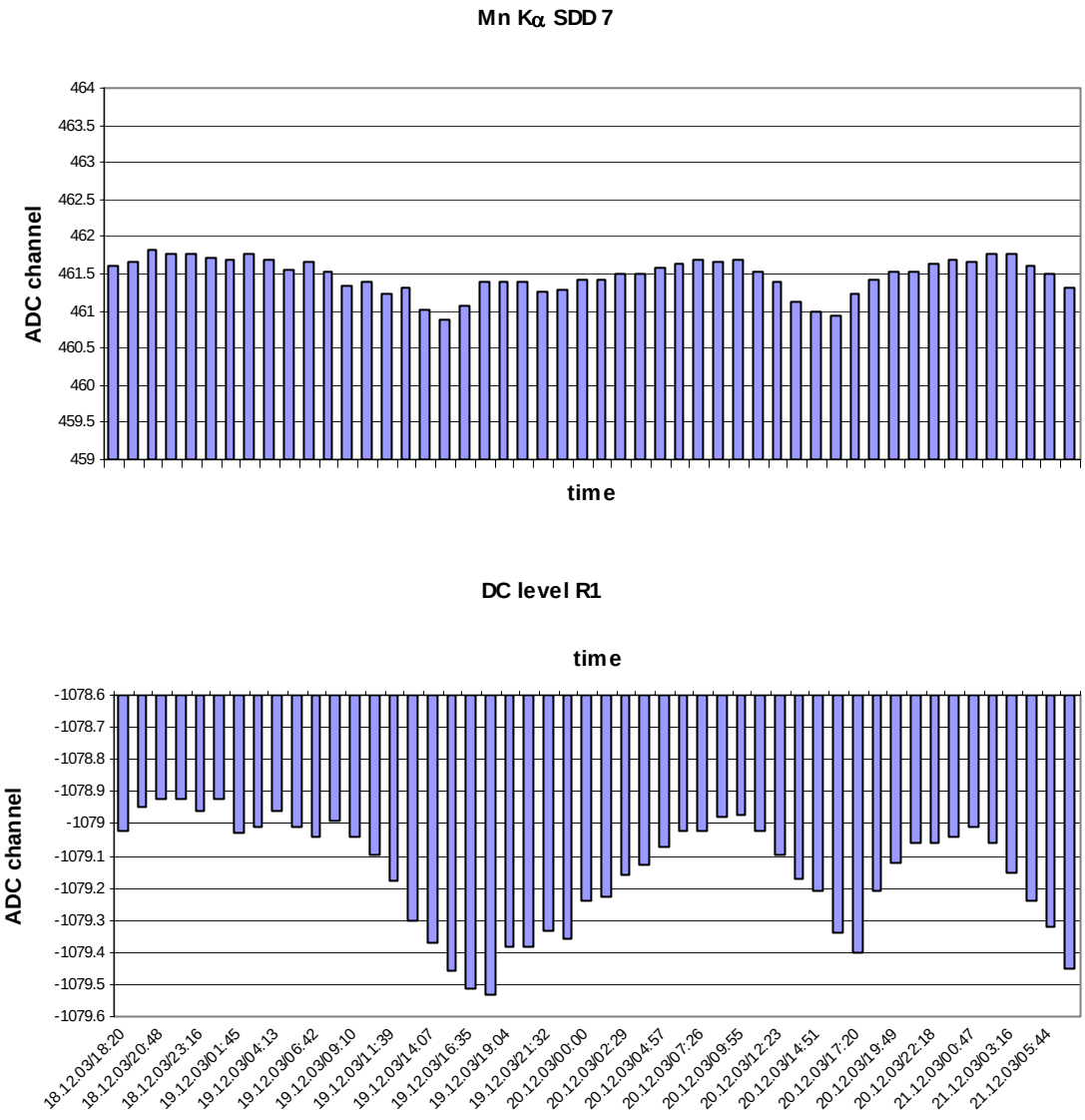

Fig. 5 Mn Kα peak position on SDD 7 and R1 bias voltage, with new filter on R1

The conclusion we drawn from this measurement was that R1 does not produce the gain variation, but both R1 and output FET are influenced by the same instability on some other element. The inverted dependence on R1 after replacing the filter was due to HV residual current redirection trough R1 supply.

Two hypotheses directly connected to the measurements were done; the first assumes instabilities on the HV chain, and the second attributes some residual influence to the reset diode, connected to R1. Since none of them seem plausible (HV has a weak correlation with the gain and R1-reset bias variation was reduced by an order of magnitude without gain stability improvement), an indirect, third hypothesis, would be to assume a connection with the back voltage (correlated with gain), due to the fact that back and HV are powered by the same supply, trough separate dividers.
Indeed, the first test done by decoupling R1 and the 2 reset diodes demonstrated that last ones, after negative polarization, have no influence on gain (same level of fluctuation).

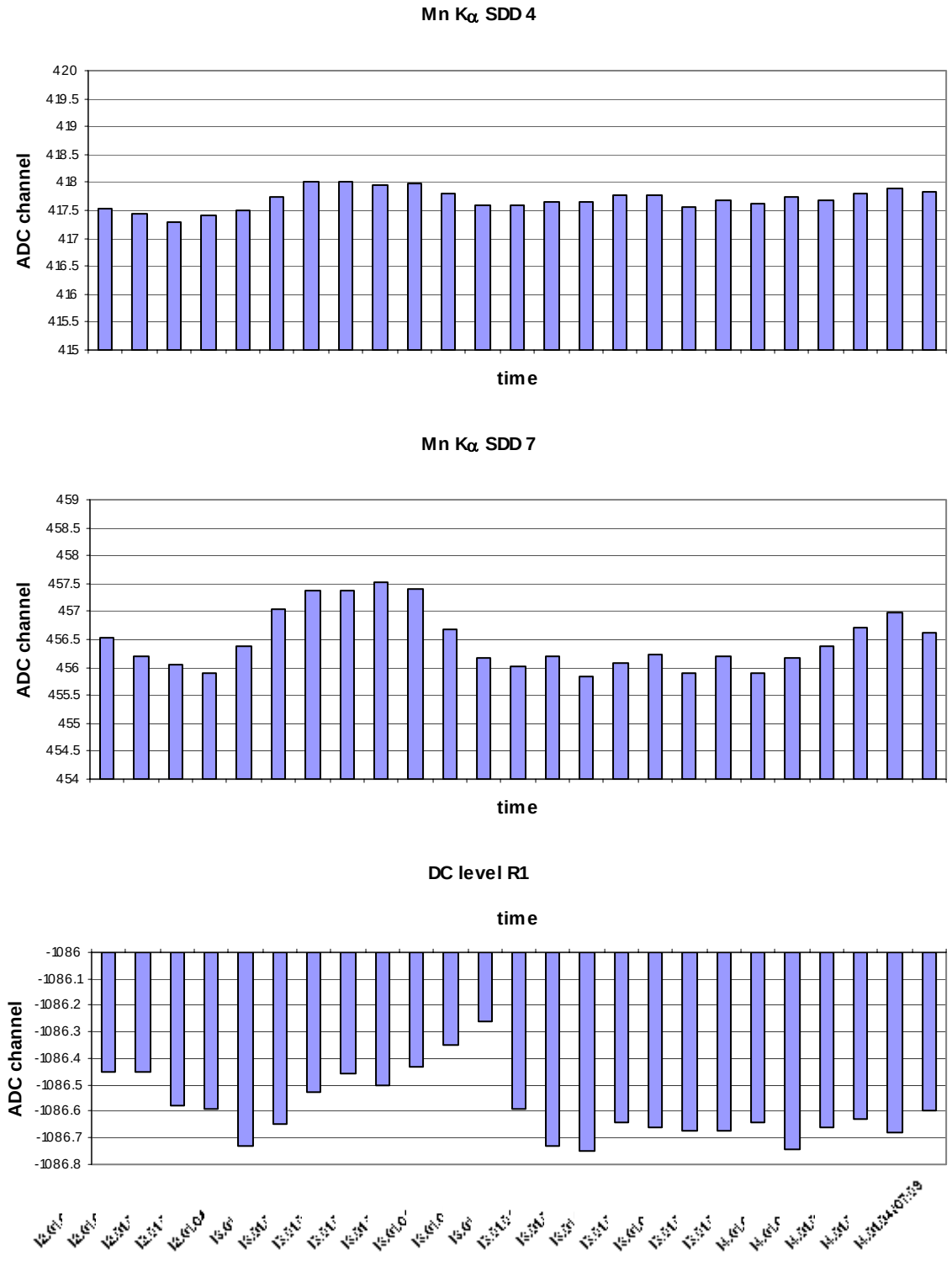

Fig. 6 Mn Kα peak position SDD4&7 and R1 bias voltage (R1 and reset supplies separated)

The first step in checking the HV and Vback influence was adding them in the acquisition.

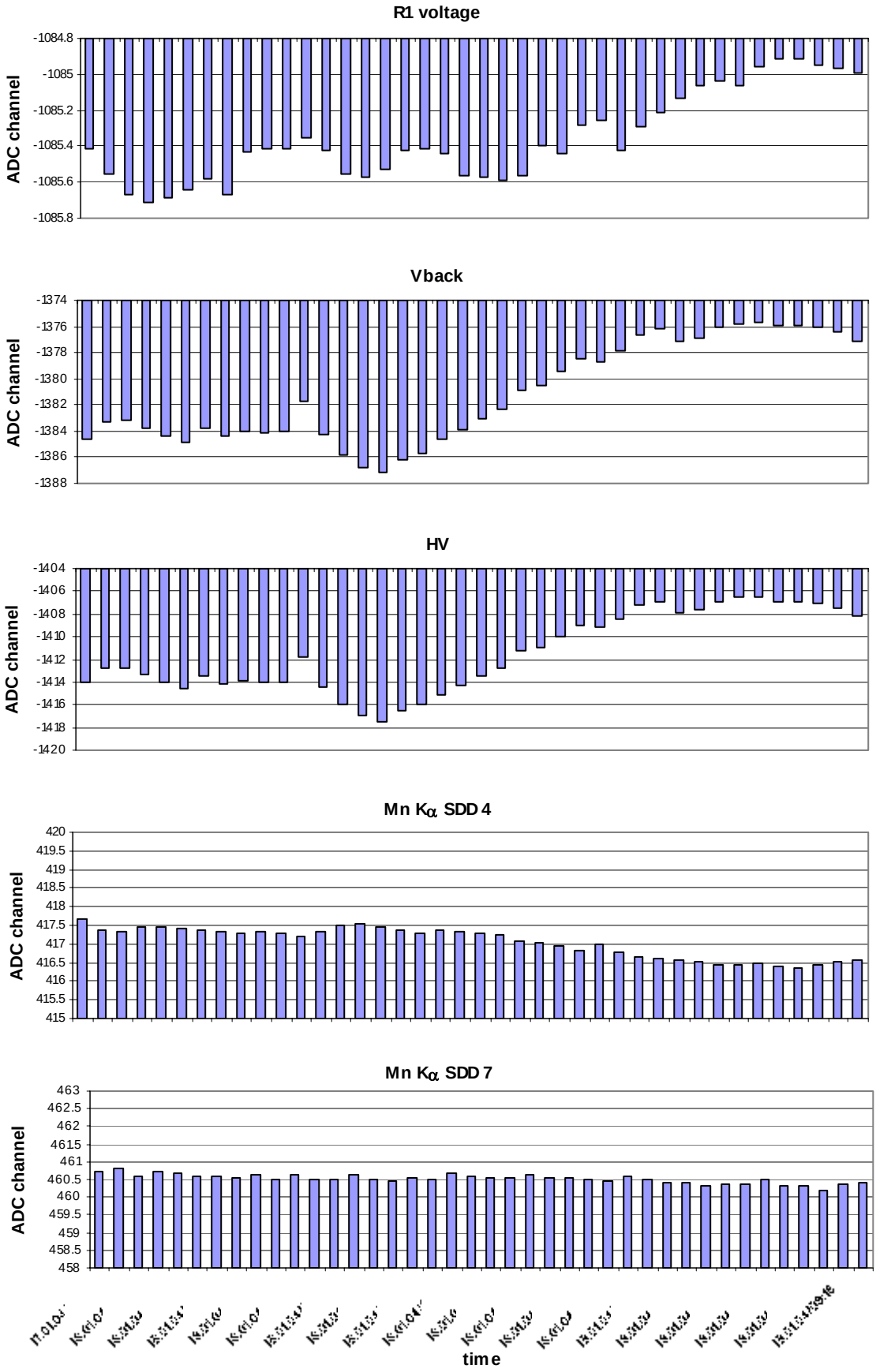

Fig. 7 Mn Kα peak position for SDD 4 and 7 and voltages on R1, HV, Vback

As can be seen, all graphs are correlated. This is due to relatively high current driven by HV dividers on the 7 SDDs, to be summed with the external divider current for HV and Vback, resulting in a total consumption of about 2 mA. Conventional HV power supplies exhibit at this consumption a stability at the level $10^{-1} \div 10^{-2}$ V, which could be further reduced at pin level by the resistive part of the filters impedance and the non-linear voltage-current behavior of the MOS chain. The resistive voltage divider/regulator may also constitute a problem in case of small impedance variation of the internal divider.
Indeed, by replacing the HV CAEN power supply with another one built with a standard HV stabilizer (VB408), the results get worst (not reported here), showing that the stability of the HV (Vback) bias voltages is relevant.
Since chips better than VB408 are hard to be found on the spot market, the first step in improving the Vback supply stability (considered more critical) consisted in a series connection of 4 low voltage stabilizers. The resistive dividers were eliminated, each voltage being tuned directly from the stabilizer. A slight improvement of gain stability was seen.

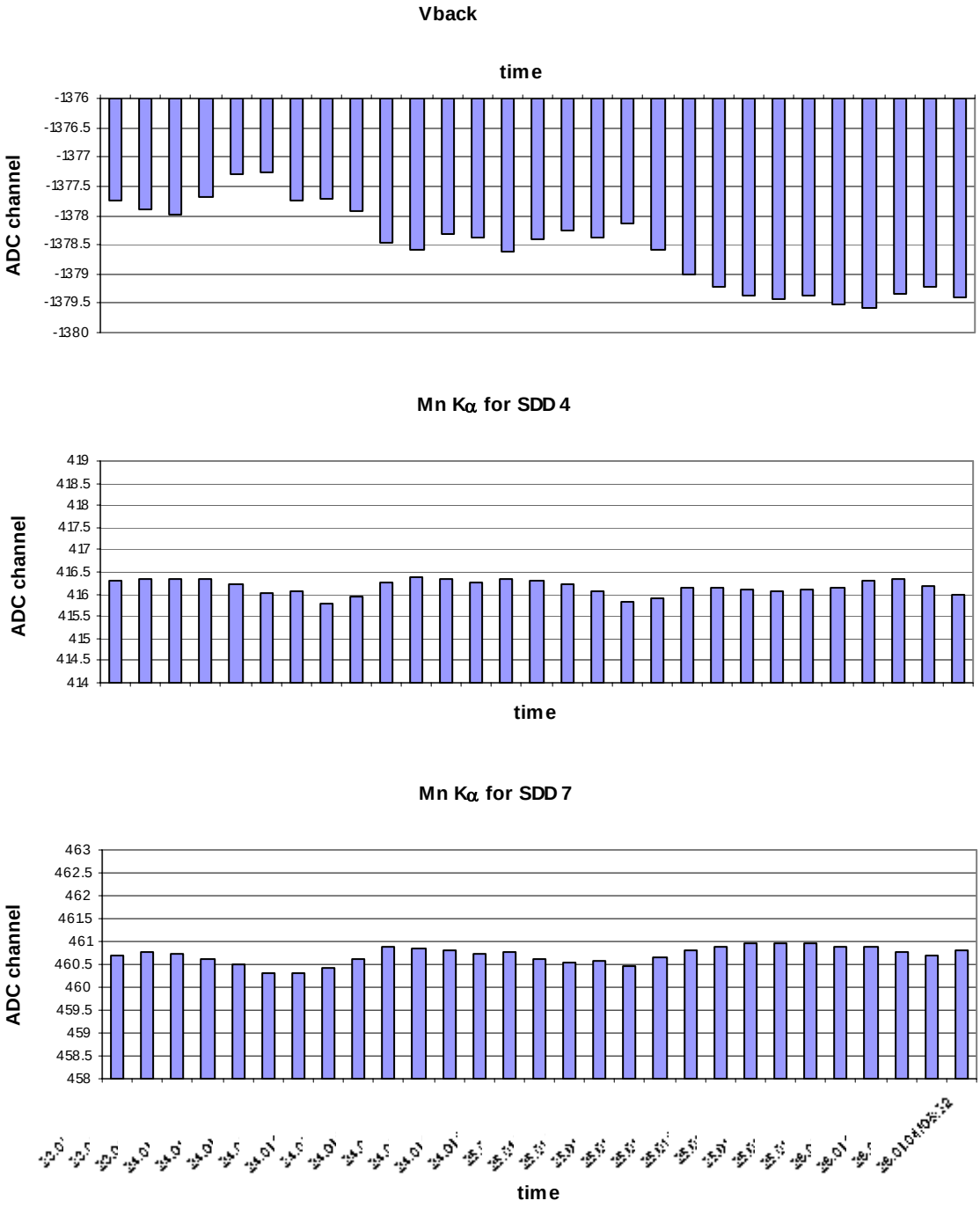

Fig. 8 Mn Kα peak position for SDD 4 and 7 and Vback with the low-voltage stabilizers

One can observe that the gain range reduction is not linearly dependent on Vback range reduction, due to the non-linear dependence between the two magnitudes. A short-range scan of these two correlated parameters is shown in the Fig 9.

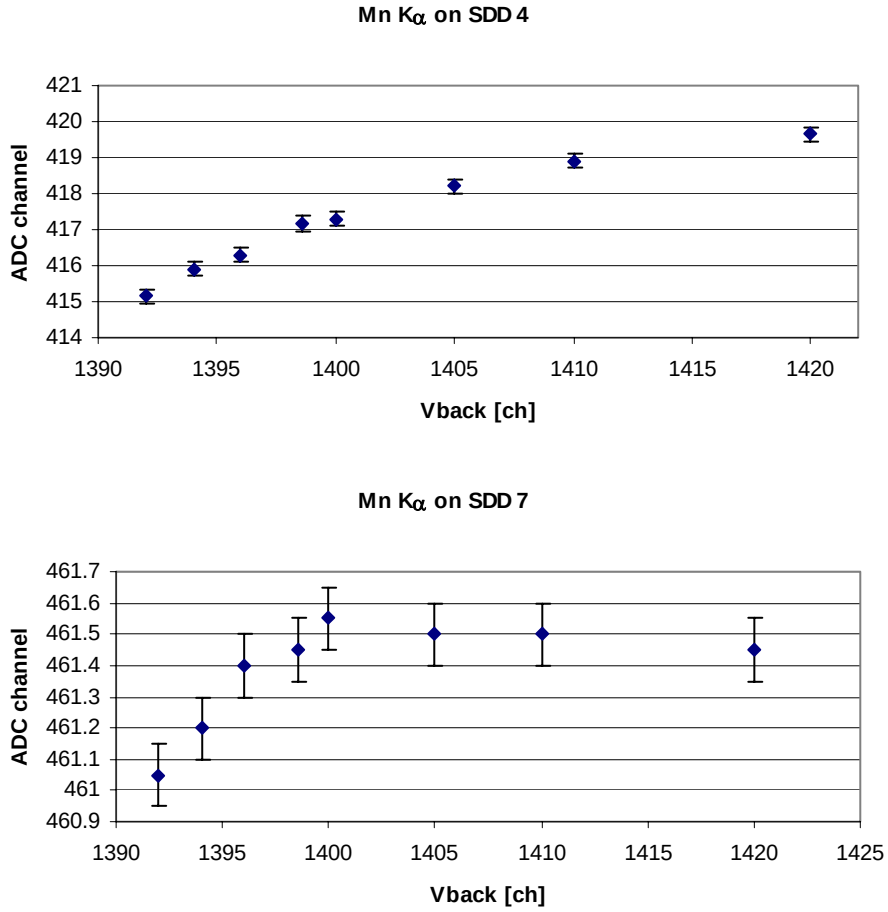

Fig. 9 Mn Kα peak position for SDD 4 and 7 as a function of Vback

The conclusion is that more precise power supplies are required. The solution adopted was a software-controlled PS unit. The online measured values for HV and Vback (14-bit resolution) were used to create two feedback voltages as output of the available programmable DACs (16-bit resolution). These voltages were applied to the stabilizer external reference, to compensate the fluctuations with respect to the set points. The redundancy in the DAC resolution ensures the coverage of a wide range, allowing fixing also the set point via software (80-120 V, in our case). The precision obtained by stabilizing this way HV and Vback was 3 mV, which represents a major improvement with respect to the previous supply units. The coupling of the DAC to the reference circuit, which is polarized at negative values, was done using a photoresistive optocoupler (Fig 10).

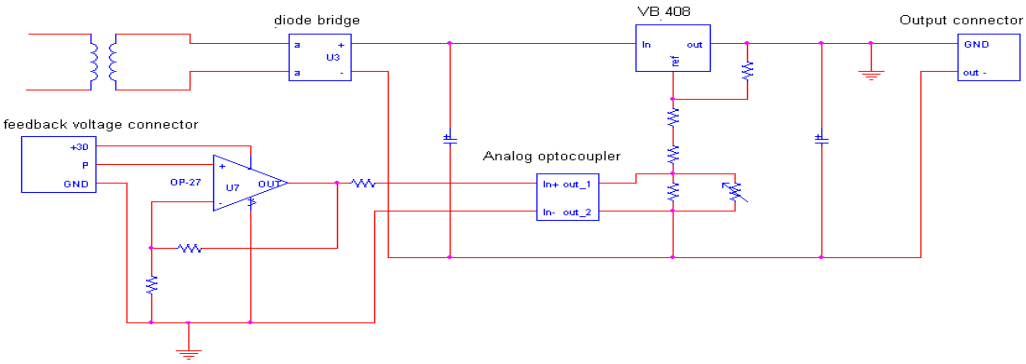

Fig. 10 The HV feedback circuit

The result of last changes was reaching the desired level of stability (below 2 eV) for the present phase of development of a prototype setup.

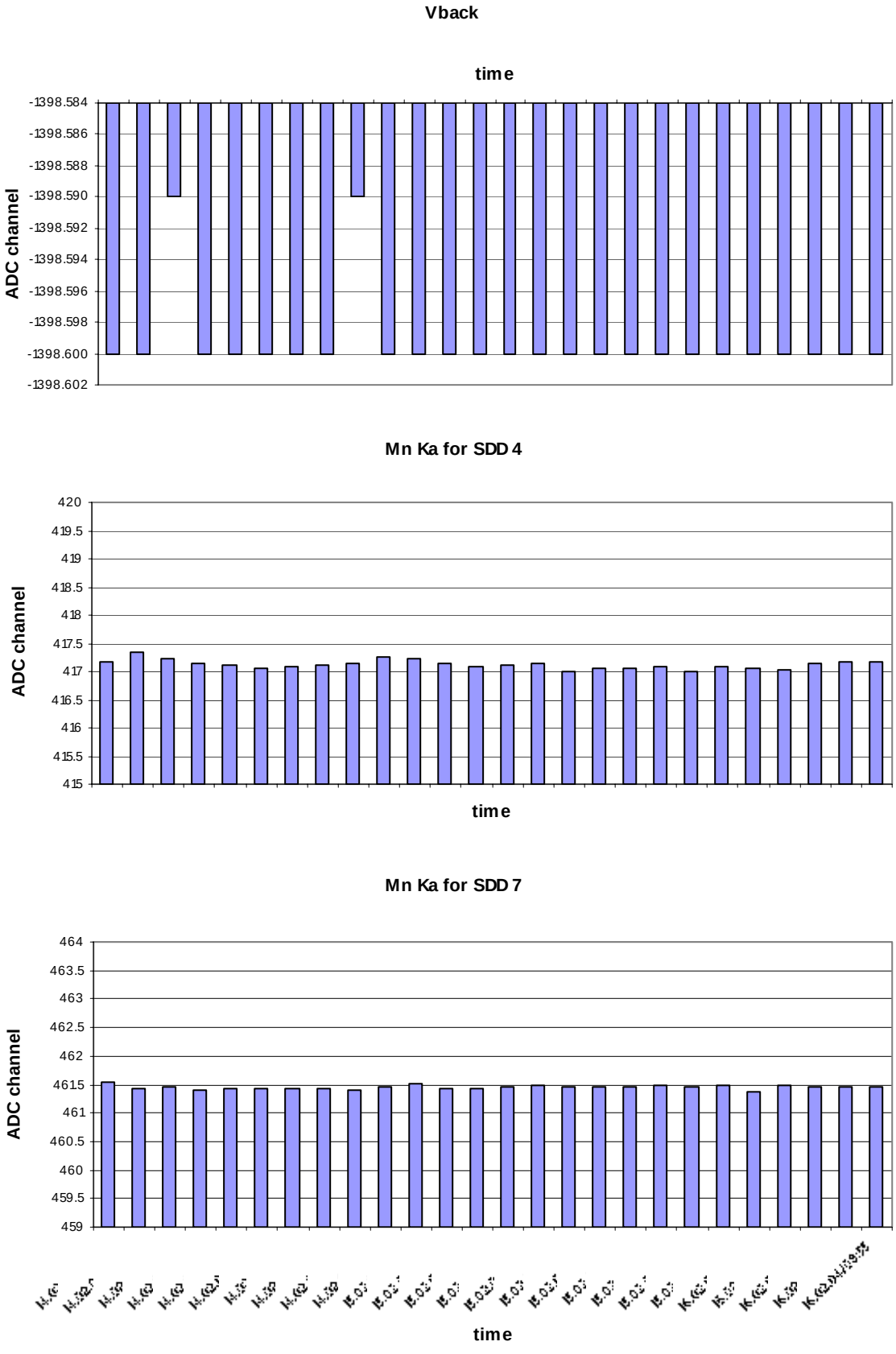

Fig. 11 Mn Kα peak position for SDD 4 and 7 and Vback with software stabilization

The achieved result allowed us to perform more precise linearity tests on the 2 stabilized devices. A set of measurements, on which the SDDs were exposed to fluorescent X-rays from various excited metals, ranging from 4.9 to 15 keV, are summarized in the Fig 12.

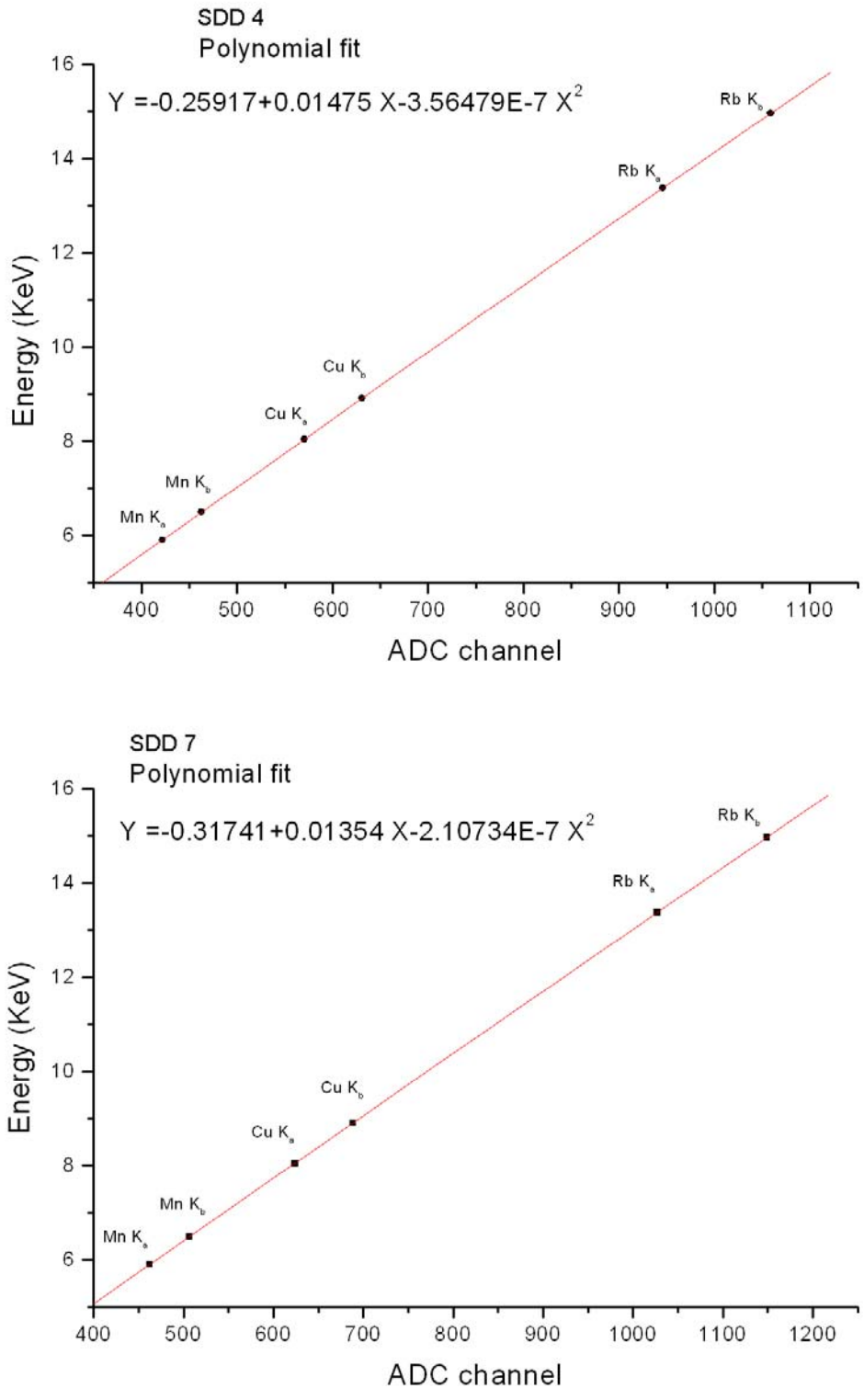

Fig. 12 Linearity measurements

Each line energy was obtained by weighting the components with their natural intensities. One can see that quadratic terms obtained from the fit are very small compared to the linear ones, resulting in an upper limit of eventual non-linearity in the ROI (6-8 keV) below 0.2 eV, (actually smaller than the achieved device stability).

A second test performed on the SDD 4 and 7 concerned the response at high rate of background.
Comment: due to the nature of estimated background in DAFNE IR, consisting in charged particles lost from the primary beams via Touschek effect, we refer as high-rate background events with moderate hit rate but high energy deposition (resulting in high energy deposition rate), rather than a high rate of X-ray hits. The difference between the two might influence the output FET pileup-reset regime.
A β-emitter (Sr^{90}) with a continuous spectrum ranging up to 2.27 MeV was used to produce a background flux of ionizing particles. The signal (Mn K and Rb K) rates were below 10 Hz/SDD. The source activity and the detector solid angle limited the rate of background hits at 200 Hz/SDD. The energy deposition spectra is to be calculated via Monte Carlo technique, however, most of the hits produced by the Sr^{90} emission deposited more energy than a minimum ionizing particle, which constitute an important fraction of machine background. A small shift of the calibration lines was observed, which might be associated to the effect of the ionizing particle background. However, further investigation is necessary in order to probe the effect with higher accuracy and to check for eventual deviations due to electronics. To be mentioned that the rate used corresponds to a high level of background in the expected machine conditions. The new 30 mm^2 SDD will be essential for scanning a wider range of background rates.

Sources	Mn Kα	Er	Mn Kβ	Er	Rb Kα	Er
Fe-Rb SDD 4	421.7	0.0091	462.6	0.026	946	0.0041
Fe SDD 4	421.7	0.0132	462.5	0.035		
Fe-Rb-Sr-SDD 4	422.5	0.0035	462.8	0.15	947.1	0.287
Fe-Rb SDD 7	462	0.0093	506.3	0.025	1027	0.041
Fe SDD 7	461.9	0.014	506.3	0.036		
Fe-Rb-Sr-SDD 7	462.2	0.032	506.3	0.12	1028	0.26

Table 1 Effect of the 200 Hz background (Sr measurement) on the Mn and Rb K lines determination

Bibliography

1. SIDDHARTA IR-1