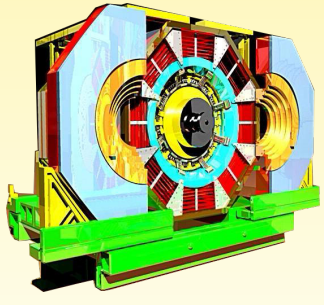
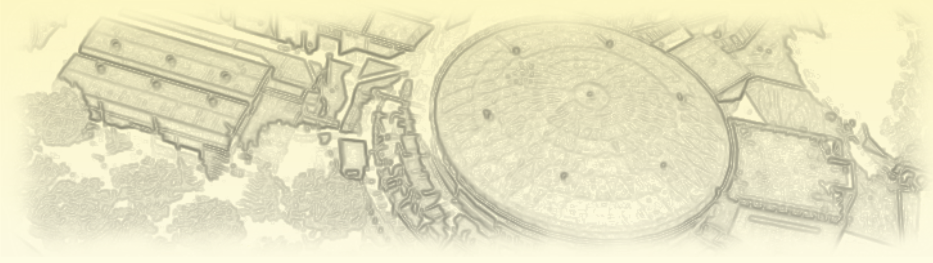
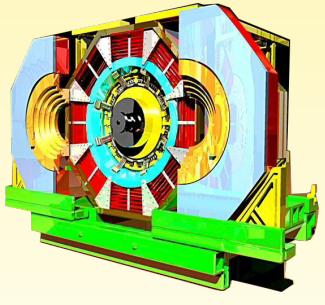
Study of a zero degree radiative photons tagger for ISR events in BESIII



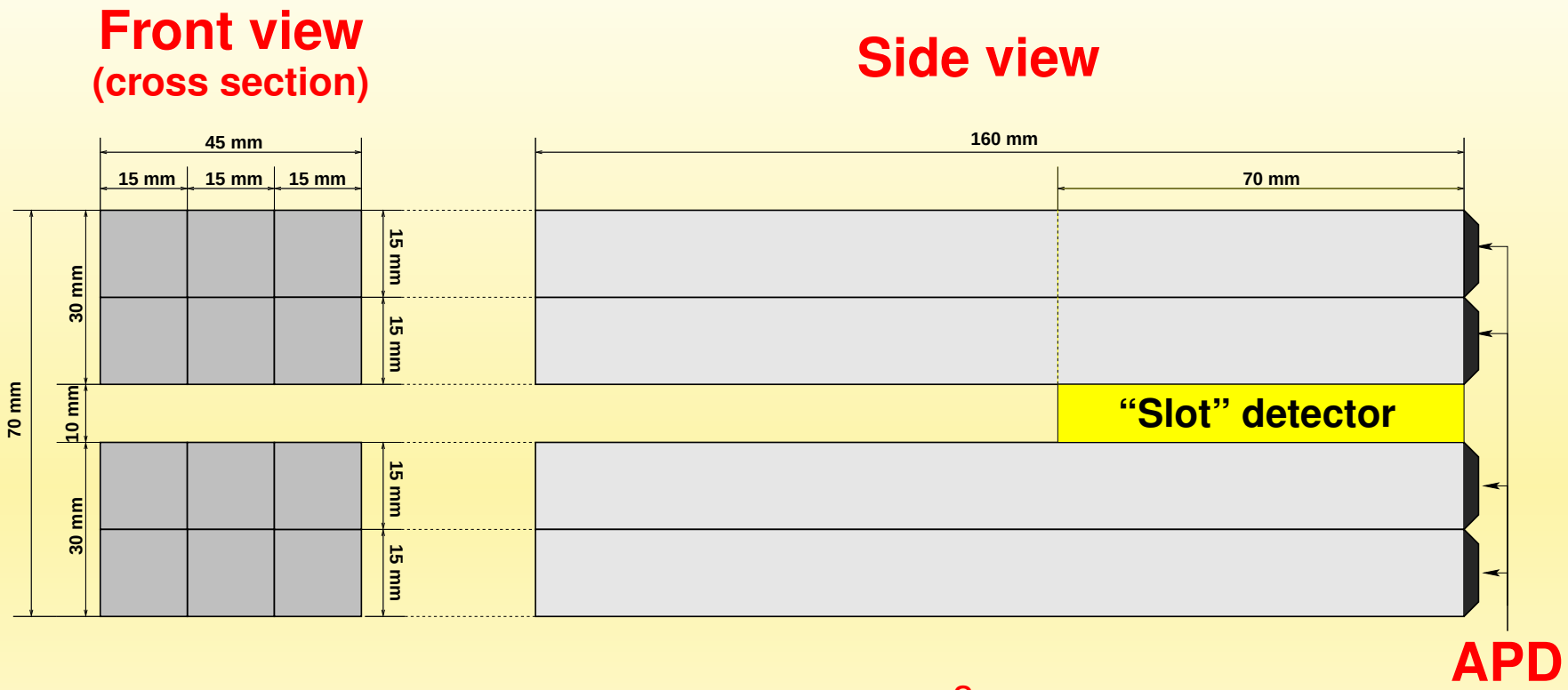




Outline

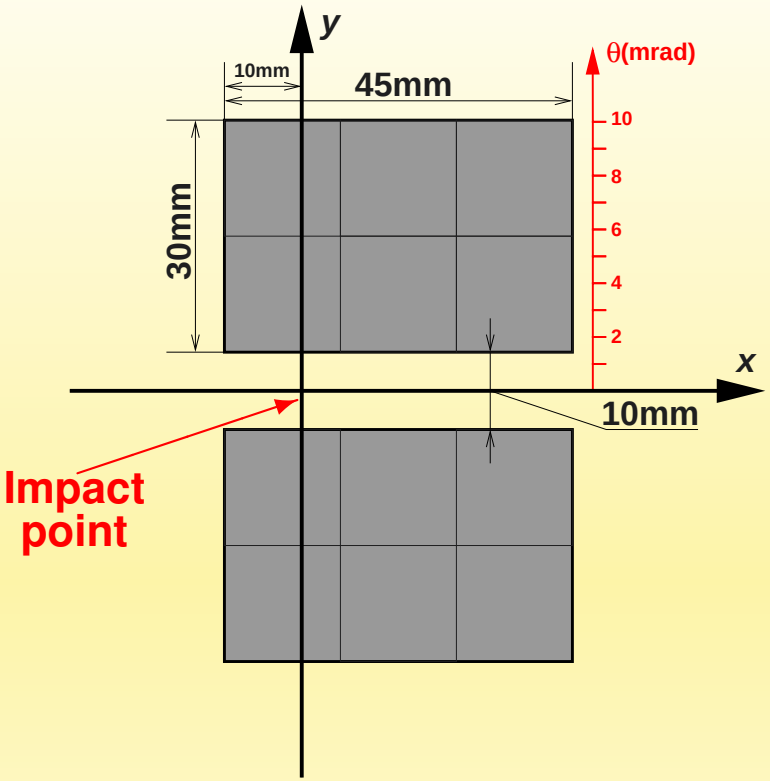
- Zero degree detector (ZDD) drawing
- Simulation of Bremsstrahlung process: $e^+e^- \rightarrow e^+e^-\gamma$
- ZDD performances with LYSO crystal

Design



- Two 3×2 matrices of $1.5\times1.5\times16$ cm^3 of LYSO bars
- Total volume 864 cm^3
- Readout with 24 APDs
- Possible Luminosity-monitor "Slot" detector in the last 7 cm

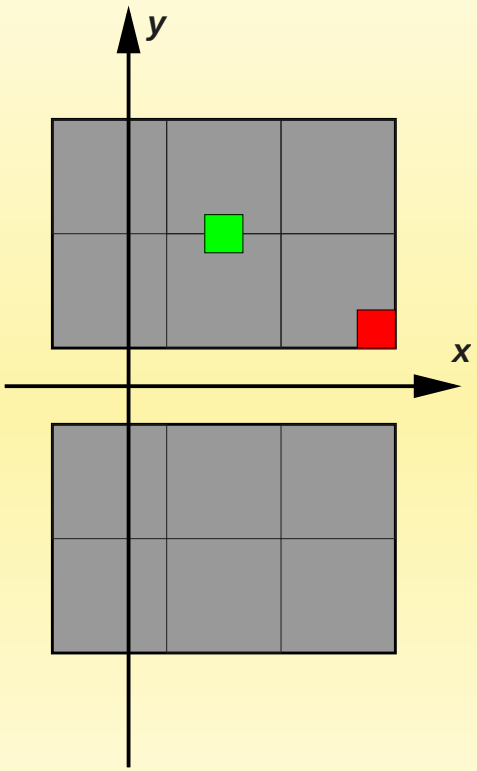
Bremsstrahlung simulation



- $E_{\text{beam}} = 1.89$ GeV
- $E_{\gamma}^{\text{min}} = 50$ MeV
- $\sigma_{\text{Bremss.}}(4\pi) = 353$ mb
- $\sigma_{\text{Bremss.}}(\text{ZDD}) = 10$ mb
- $\mathcal{L} = 8 \times 10^{32}$ cm^{-2} s^{-1}

- ISR in ZDD 13.7% of total solid angle
- Bremsstrahlung in ZDD 2.8% of total solid angle
- Bremsstrahlung rate in ZDD:
  1.5 MHz at $\mathcal{L} = 3 \times 10^{32}$ cm^{-2} s^{-1}
  3.9 MHz at $\mathcal{L} = 8 \times 10^{32}$ cm^{-2} s^{-1}

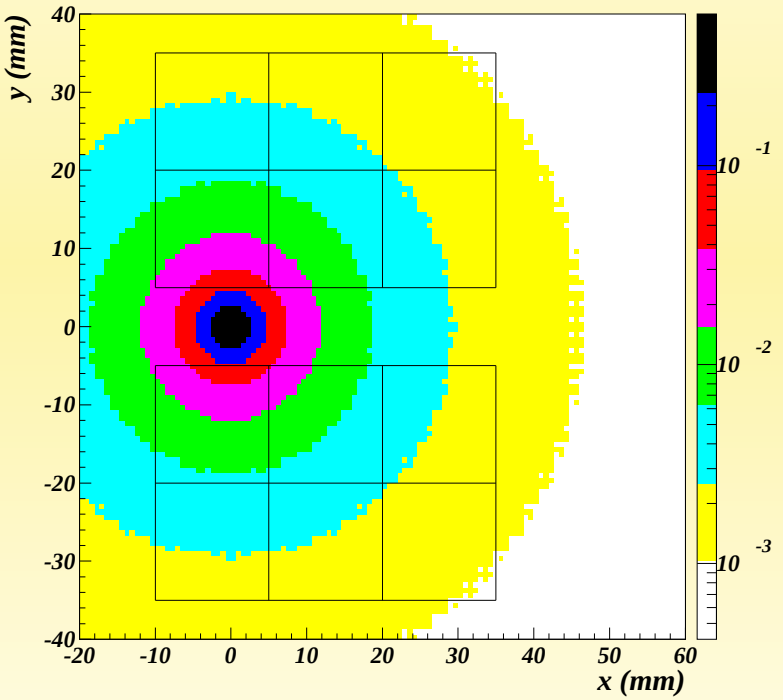
Energy resolution$_1$



E_γ (GeV)	$\sigma_{E_\gamma}/E_\gamma$ Central (green square)	$\sigma_{E_\gamma}/E_\gamma$ Edge (red square)
1.0 - 1.4	3.6%	26.0%
0.2 - 0.4	4.9%	32.0%
0.2 - 1.4	4.1%	26.7%

Energy resolution$_2$, the ISR case

ISR photon angular distribution on the ZDD



E_γ (GeV)	$\sigma_{E_\gamma} / E_\gamma$
1.0	7.9%
0.5	9.5%

Physical properties of LYSO

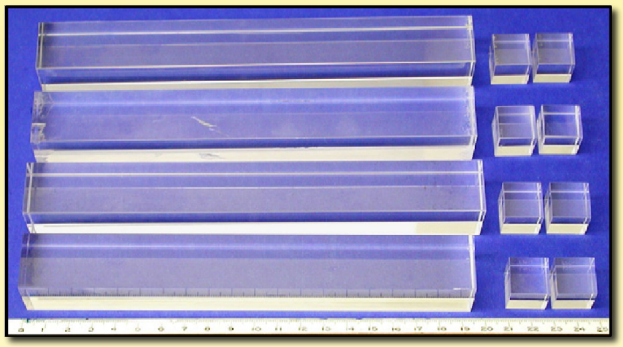
LYSO (Cerium-doped Lutetium Yttrium Orthosilicate)

Density (g/cm^3)	7.4
Effective Atomic Number	66
Radiation Length (cm)	1.1
Molière Radius (cm)	2.0
Decay Constant (ns)	40-44
Peak Emission (nm)	428
Light Yield (BGO=1)	1.9
Index of Refraction	1.82
Peak excitation (nm)	375
Radiation Hardness (rad)	$> 10^6$
Hardness (Mohs)	5.8
Hygroscopicity	No

- High light output (L.O.)
- High density
- Quick decay time
- Good energy resolution
- High radiation hardness:
  $\sim$10% L.O. loss after 1 Mrad

ZDD Components

LYSO crystals readout by APDs



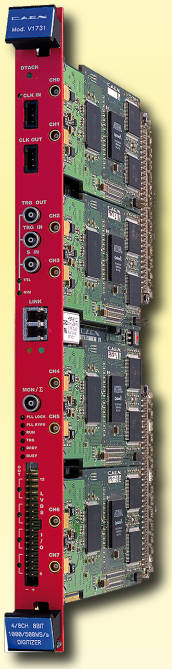
LYSO Crystals

APD

Possible readout electronics

Flash ADC

(CAEN V1731)



- 8/4 channel
- 8 bit 500 MS/s - 1 GS/s (interleaved) ADC
- 1 Vpp Input dynamics (single ended or differential).
- External ADC clock input or PLL synthesis from internal/external reference
- Front panel clock In/Out available for multiboard synchronisation (direct feed through or PLL based synthesis)
- 16 programmable LVDS I/Os
- Trigger Time stamps
- Memory buffer: up to 4 MSample/ch
- FPGA for real-time data processing
- Zero Suppression and Data Reduction algorithms
- Programmable event size and pre-post trigger adjustment
- VME64X compliant interface
- Optical Link interface
- A2818 PCI controller available for handling up to 8 Modules daisy chained via Optical Link