BESIII Cylindrical GEM IT Project for BESIII

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(LNF-INFN)
Outline

• Purpose of this work
• Mechanics issues
• Cosmic ray setup
• Plans for the frontend electronics
• Writing a Conceptual Design Report
Gain change over 2009-2013 with Bhabha events

- Compared with 2009, now the gas gains of first 5 layers decrease about 26% —14%
- The gains of the first 10 layers show an obvious decrease
- The gains of the layers in the outer chamber show no change
A new inner drift chamber is under construction, and will be finished in next April.

A different end plate is used, to shorten the wire length and reduce backgrounds.

The new inner drift chamber will be installed in 2015 but an expected luminosity doubling jeopardizes its lifetime.
CGEM detector for BESIII

Three active layers

Active area
- L1 length: 532 mm
- L2 length: 690 mm
- L3 length: 847 mm

Inner radius: 78 mm
Outer radius: 178 mm

Requirements

- Rate capability: $~10^4$ Hz/cm$^2$
- Spatial resolution: $s_{xy} = ~100\mu m$ : $s_z = ~1mm$
- Momentum resolution:: $s_{pt}/P_t = 0.5\%$ @1GeV
- Efficiency = $~98\%$
- Material budget <= 1.5% all layers
- Coverage: 93% 4$\pi$
- Operation duration ~ 5 years
A CGEM detector has been added to the BESIII simulation in order to preliminary evaluate its possible performance.

A lot of details in the simulation.

Reconstruction code needs to be developed to fully evaluate the impact on the physics.
CGEM point resolution vs. B

**Readout**

<table>
<thead>
<tr>
<th>Type</th>
<th>Resolution $\sigma_{r\phi}$ ($\mu$m)</th>
<th>Resolution $\sigma_z$ ($\mu$m)</th>
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<tbody>
<tr>
<td>Digital readout</td>
<td>330</td>
<td>400</td>
</tr>
<tr>
<td>Analog readout</td>
<td>80</td>
<td>150</td>
</tr>
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</table>

* Analog readout uses magnetic field effect avoidance.*

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A. Calcaterra, for BESIII-Italy

BESIII Physics Workshop, IHEP 2013-09-22
CGEM expected performance

CGEM inner detector  (Vs MDC inner detector)

- **Improves dz resolution significantly** (by a factor of 2.6~6)
- **Comparable dr resolution** (~5% poorer for low momentum tracks)
- **Comparable momentum resolution** (~5% better for high momentum tracks)
First layer: construction goals

- Design, construction and test of a CGEM prototype, in case first layer of a new CGEM Inner Tracking

- Design, construction and test of an analog readout system to achieve $< 100 \, \mu m$ xy and $< 200 \, \mu m$ z resolutions

- Budget (euros) requested to Foreign Affairs Ministry, following the Agreement of scientific cooperation for a Joint laboratory “INFN-IHEP”

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<tr>
<th></th>
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<tr>
<td>Italian Ministry of FA expenditure</td>
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<tr>
<td>Foreign Institution expenditure</td>
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<td>More funds</td>
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<td>0%</td>
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<tr>
<td>1st year project cost</td>
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</table>
The path toward a CGEM-IT

Much effort needed to go from one layer to the complete IT

- R&D program (Jun 2013 – Jun 2014)
- First layer funded under the MAE agreement
  - design (Sep-Nov 2013)
  - construction (May 2014 – Jul 2015)
- Write a Conceptual Design Report (CDR) (winter 2013/spring 2014)
- Submission of the CDR to BESIII for approval (June 2014).
- Second layer
  - design (Dec 2013 – Mar 2014)
  - construction (Feb-Nov 2015)
- Third layer
  - design
  - construction (Jul 2015 – Mar 2016)
- Test and integration (Jan-May 2016)
- Ready for installation (Jan 1st 2017)
First mechanical drawings (Fe)
We had a first interaction with Chinese engineers to understand the mechanical constrains for the inner tracker.

- Doable but very limited space.
- The beam pipe support closes most of the space in the z direction.
- The KLOE2 design needs modification.
We plan to use three layers of the same length in order to facilitate the mechanics of the installation and the robustness of the structure.

For the two innermost layers the electronics will be placed inside the gaps between the chambers.

The design for the outermost layer will be evaluated after a meeting with BESIII people scheduled tomorrow.
Preliminary solid model of the cathode has been done and it is currently under discussion within the collaboration.

Space for housing the HV connectors

positioning holes
CGEM layer design

- 3D model of the one of the cylindrical GEM layer showing the internal and external rings.

inner ring on one side

outer ring on the other side
The anode conceptual design

The anode design will be finalized once the studies with simulations and planar prototype will be finished (May 2014).

Nevertheless we need to address many mechanical constraints now to be sure that our design will match perfectly other parts of the detector.
Anode simulation

- Due to diffusion the charge cloud collected on the readout board is bigger than the strip width and a weighting method is used for calculate the exact track position in two dimensions.

- A simulation (performed with ANSYS Maxwell) is under way to study the couplings both between the strip planes and between a strip plane and ground.
- Any chance to reduce the capacitance will be investigated.
- The deadline for this task is May 1st 2014.
Section of the assembly
One-layer assembly
Before freezing the design

• Rohacell based fake cathode to be done in Ferrara (end of September).
• Discuss mechanical constraints with Chinese engineers (we have two days of meetings at IHEP on the 25th-26th).
• Evaluate the space needed the HV, signal and gas connectors, and cooling tubes.
• Evaluate FE board dimensions, concurrently with final anode design (will be done in 2014).
Tooling for detector construction

- The proper tooling for cathode and GEM layers construction has been designed.
- Assembly procedures have been discussed.
- Manpower needed for construction and assembly has been evaluated.
- We will reuse as much as possible the tooling and the expertise from KLOE2.
- Careful review of the tooling design is under way (very important since the procurement of the material will start soon).
Mold positioning
The cathode assembly tooling and procedure

Position vetronite rings
Glue and machine the Rohacell structure
The cathode assembly tooling and procedure

Complete support structure
The cathode assembly tooling and procedure

Glue the cathode sheet
The cathode assembly tooling and procedure

Glue the GEM 1 supporting ring
### Schedule for detector construction

#### Task 1: R&D
- **1.1** FE - Phoswich fake cathode
- **1.2** FE - Assembly tests with Klue molds
- **1.3** FE LNF - Anode Simulation
- **1.4** LNF - Anode finalization and design

#### Layer I
1. **2.1** FE - Technical design
2. **2.2** Material procurement
   - 2.2.1) Molds
   - 2.2.2) GEM foils
   - 2.2.3) Anode
   - 2.2.4) Other material
3. **2.3** FE - Cathode construction
4. **2.4** LNF - GEM assembly
5. **2.5** Anode assembly
6. **2.6** LNF - Assembly QA and validation
7. **2.7** LNF - Full detector assembly
8. **2.8** LNF - Detector test and QA

#### Layer II
1. **3.1** FE - Technical design
2. **3.2** Material procurement
   - 3.2.1) Molds
   - 3.2.2) GEM foils
   - 3.2.3) Anode
   - 3.2.4) Other material
3. **3.3** FE - Cathode construction
4. **3.4** LNF FE - GEM and anode assembly
5. **3.5** LNF - Assembly QA and validation
6. **3.6** LNF - Full detector assembly
7. **3.7** LNF - Detector test and QA

#### Layer III
1. **4.1** FE - Technical design
2. **4.2** Material procurement
   - 4.2.1) Molds
   - 4.2.2) GEM foils
   - 4.2.3) Anode
   - 4.2.4) Other material
3. **4.3** FE - Cathode construction
4. **4.4** LNF FE - GEM and anode assembly
5. **4.5** LNF - Assembly QA and validation
6. **4.6** LNF - Full detector assembly
7. **4.7** LNF - Detector test and QA

#### Milestones:
- **CDR approval by the BESIII collaboration**
- **R&D**

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A. Calcaterra, for BESIII-Italy

BESIII Physics Workshop, IHEP 2013-09-22
The planar prototype
CGEM first layer: cosmic test setup (LNF-FE-TO)

- The COMPASS-type readout layer is substantially different from the KLOE2 one
- It must be tested, before employ in a full-scale cylindrical prototype
- KLOE2 cosmic-ray telescope borrowed
  (3 complete and working planar GEM chambers of KLOE2 type)
- To these we will add a small (10x10 cm²) planar chamber with GEMs, and a COMPASS-type readout layer
- Planar GEM chamber kit from CERN ordered and arrived in LNF
- Build, test and operate setup, to characterize COMPASS-type readout
- Start taking cosmic data, beam if possible
- Small rate if few channels: will take time
Schedule for planar prototype

1. Planar Prototype
   - 1.1) Procurement: 64 days
   - 1.2) LNF - Chamber assembly: 44 days
   - 1.3) LNF - RX test: charge sharing: 44 days
   - 1.4) LNF - cosmic ray setup - hardware: 43 days
   - 1.5) FE/LNF - cosmic ray setup - DAQ and software: 142 days
   - 1.6) LNF - DAQ system for test chamber: 65 days
   - 1.7) FE/LNF - Cosmic ray tests: 20 days
   - 1.8) FE/LNF - Beam test and data analysis: 14 days
Plans for electronics design
CGEM IT FrontEnd electronics

- Readout ASIC for CGEM:
  - Modify/adapt the existing TOF-PET ASIC (Rolo, Rivetti et al. http://iopscience.iop.org/1748-0221/8/02/C02050) in IBM 130nm for PET applications

- Re-design a new analogue FE (suited for CGEM signals)

- Use of the same BackEnd of TOF-PET

- Migration to a newer and cheaper technology: IBM 130nm → UMC 110 nm should be exportable in China (implemented in Italy)

- Integration and Development of the new ASIC for CGEM
TOF-PET: Basic Features

Features of an ASIC for SiPM readout in PET applications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>64</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>80 – 160 MHz</td>
</tr>
<tr>
<td>Dynamic range of input charge</td>
<td>300 pC</td>
</tr>
<tr>
<td>SNR ($Q_{in} = 100$ fC)</td>
<td>&gt; 20-25 dB</td>
</tr>
<tr>
<td>Amplifier noise (in total jitter)</td>
<td>&lt; 25 ps (FWHM)</td>
</tr>
<tr>
<td>TDC time binning</td>
<td>50 ps</td>
</tr>
<tr>
<td>Coarse gain</td>
<td>$G_0$, $G_0/2$, $G_0/4$</td>
</tr>
<tr>
<td>Max. channel hit rate</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Max. output data rate</td>
<td>320 Mb/s (640 w/ DDR)</td>
</tr>
<tr>
<td>Channel masking</td>
<td>programmable</td>
</tr>
<tr>
<td>SiPM fine gain adjustment</td>
<td>500 mV (5 bits)</td>
</tr>
<tr>
<td>SiPM</td>
<td>up to 320pF term. cap., 2MHz</td>
</tr>
<tr>
<td>Calibration BIST</td>
<td>internal gen. pulse, 6-bit prog. amplitude</td>
</tr>
<tr>
<td>Power</td>
<td>&lt; 10 mW per channel</td>
</tr>
</tbody>
</table>

⇒ GEM Input charge: 5 - 20 fC
⇒ CGEM needed time resolution ~ 1 ns
⇒ GEM Capacitance: 100-150 pF
⇒ GEM Power cons. < 7 mW

How these specs impact the choice of the readout chip architecture?
**From TOFPET to the New CGEM ASIC**

**Overview of the channel architecture**

**New FrontEnd**
- Input stage + Linear ToT

**Same BackEnd**
- but SEU Protection

**64 Channels but New Pad geometry**

- **Time** and **charge** measurements with independent TDCs
- TDC time binning **50 ps**
- Charge measured with Time-over-threshold
- Typ. power consumption is **7mW p/channel** (trigger **0.5 p.e.** w/ **SNR > 23dB** for 9 mm² MPPC, 40 KHz event rate, 1MHz DCR)
NEW CGEM ASIC: Basic Features

- UMC 110 nm technology
  (limited power consumption, to be tested for radiation tolerance)
  - Input charge: 5-20 fC
  - Sensor capacitance 100-150 pF
  - Input rate (single strip): 7-15 kHz
  - Time and Charge measurements by independent TDCs
  - TDC time binning > 50 ps \(\implies\) CGEM needed time resolution \(\sim\) 1 ns
  - Double threshold discrimination
  - Time over Threshold (ToT) to measure the charge \(\implies\) CGEM: Linear ToT
  - Power consumption < 7 mW/channel \(\implies\) 4 mW/channel feasible
High Voltage distribution

<table>
<thead>
<tr>
<th>layer (single CGEM)</th>
<th>macro-sectors</th>
<th>micro-sectors</th>
<th>micro-sector capacitances</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
<td>40</td>
<td>4.5 nF</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
<td>80</td>
<td>4.3 nF</td>
</tr>
<tr>
<td>3</td>
<td>9</td>
<td>90</td>
<td>4 nF</td>
</tr>
</tbody>
</table>

1 macro-sector = 10 micro-sectors

- HV tails have 10 conductive through-holes to bring lines on the connector side
- Resistance of the conductive glue is checked with Ohmeter (must be < 3Ω)

Macro-Sector with 10 Sectors

bottom-GEM connection
top-GEM connections
through holes
soldered connector

HV distribution block diagram (KLOE - G. Morello)
### Schedule for electronics

#### 1) Electronics

- **1.1) ASIC**
  - 1.1.1) TO - Prototypes and test
  - 1.1.2) TO - ASIC production and QA
- **1.2) TO/ LNF - on detector boards preliminary study**
- **1.3) TO - ASIC boards on detector**
- **1.4) LNF - ReadOut boards (ROBs)**
- **1.5) LNF - Transition boards (TBs)**
- **1.6) LNF - ReadOut crates (ROCs)**
- **1.7) LNF - Concentrator board**
- **1.8) LNF/FE - Preampilifier - ROB cables**
- **1.9) LNF/FE - HV system**
- **1.10) LNF/FE - HV distribution**

#### Effort

- 1) Electronics: 2,239d
- 1.1) ASIC: 783d
- 1.1.1) TO - Prototypes and test: 522d
- 1.1.2) TO - ASIC production and QA: 261d
- 1.2) TO/ LNF - on detector boards preliminary study: 108d
- 1.3) TO - ASIC boards on detector: 255d
- 1.4) LNF - ReadOut boards (ROBs): 260d
- 1.5) LNF - Transition boards (TBs): 109d
- 1.6) LNF - ReadOut crates (ROCs): 87d
- 1.7) LNF - Concentrator board: 259d
- 1.8) LNF/FE - Preampilifier - ROB cables: 109d
- 1.9) LNF/FE - HV system: 64d
- 1.10) LNF/FE - HV distribution: 205d
The Conceptual Design Report
Plan for the CDR

• During the last BESIII-Italy meeting (4 and 5 Sep. 2013) we dedicated a full session to the planning of the CDR.

• The CDR will be submitted to BESIII some time before the June 2014 Collaboration Meeting

• We expect from that Meeting the final go-ahead to proceed with the construction plan

• A detailed Table of Content has been prepared, discussed with Chinese colleagues and approved.
Sharing the effort

1. Introduction
   1. The present BESIII Inner Tracker
   2. Luminosity Issues
      1. Present and expected backgrounds
   3. Inner Tracker Upgrade Requirements

2. Detector design
   1. Operating principle of a triple Cylindrical GEM detector
      1. The KLOE2 Inner Tracker: know-how and first results
   2. BESIII CGEM innovations
      1. Rohacell
      2. Anode design
      3. Analog vs. digital, expectations and measurements

3. The BESIII CGEM-IT
   1. CGEM-IT vs DC-IT
   2. Mechanical Design
   3. Tooling and Construction

4. Simulation of Cylindrical GEM Inner Tracker
   1. Parametric Simulations (Liang)
   2. CGEM-IT full Offline Reconstruction
      1. Pattern Recognition
      2. Tracking
      3. Acceptance, Resolutions and Reconstruction Efficiencies
   3. Monte Carlo simulation results
      1. Physics Benchmark

5. Front End Electronics
   5. Requirements
      5. Power Consumption
   6. System Block Description
   7. On-Detector Electronics
      5. ASIC
   8. Off-Detector Electronics

6. DAQ and Trigger
   5. Requirements
   6. Dead time and bandwidth
   7. Possible second level trigger future upgrades
   8. Storage

7. Integration of the CGEM-IT with the Spectrometer
   5. Mechanical design
      5. Interfacing with beam pipe
      6. Interfacing with Outer DC
   6. Power Dissipation and Cooling
   7. Gas Systems
   8. HV Systems
   9. Slow Controls

8. Money, manpower, schedule, subdivision.....
Acknowledgements

• Thanks to BESIII authors of talks at the April Workshop in Frascati!
  – Dong Mingyi
  – Wang Liangliang
  – Xiu Qinglei
  – Ye Mei
• Thanks to Qun Ouyang for help in preparing the CDR!
• Thanks to G. Morello (KLOE2)
  – KLOE2 beam test data
• Thanks to Gigi Cibinetto (FE)!
  – Author of the remaining of these slides
Spares
Time-to-Digital Converter

**Analogue TDC with 50 ps time binning** - based on Time-to-Amplitude Conversion [Stevens89, Rivetti09]
- TDC Control: switching, hit validation, buffer allocation, data reg.
- Time stamp: 10-bit master clock count + Fine time measurement
TDC operation for a valid event

Current TOFPET

\[ \text{ToT (energy meas)} = t_2 - t_0 \]

A. Calcaterra, for BESIII-Italy
Floorplan of the 64-channel mixed-mode chip

- CMOS 130nm 25mm² 64-channel ASIC
- Highlight shows the allocated area for bias and calibration circuitry.
- One pad-free edge to allow abutting two twin chips into a 128-channel BGA package.
CGEM Specifications

Detector Spec

- Input charge: 5-20 fC
- Cstrip 100-150 pF
- Input rate (single strip): 7-15 kHz

Readout section

- Trigger latency: 8-9 μs - Dead time. 4 μs
- Trigger rate: 1-2 kHz

Input section (pre+shaper)

- Input impedance 120-300 Ω
- Charge sensitivity 20-40 mV/fC
- Shaping time: 50-100 ns
- ENC: 400e+40e/pF to 600e+60e/pF

Data conversion section

- Charge meas resolution: 7-8 bits
- Time meas resolution: 10-20 ns

Power consumption < 7 mW p/channel ⇒ 4 mW p/channel feasible
Manpower for the construction of one layer

From KLOE and our own evaluations

• GEM foils test (@ LNF): 1 physicist and/or 1 technician for 1 week – full time.

• GEM gluing on the molds (@ LNF): 2 or 3 phys/techs + 1 supervisor for 2 months – full time

• Cathode and anode construction (in Ferrara): 2 or 3 phys/techs + 1 supervisor for 2 months – full time

• Assembly of the detector (@ LNF): 2 or 3 phys/techs + 1 supervisor for 2 weeks – full time.