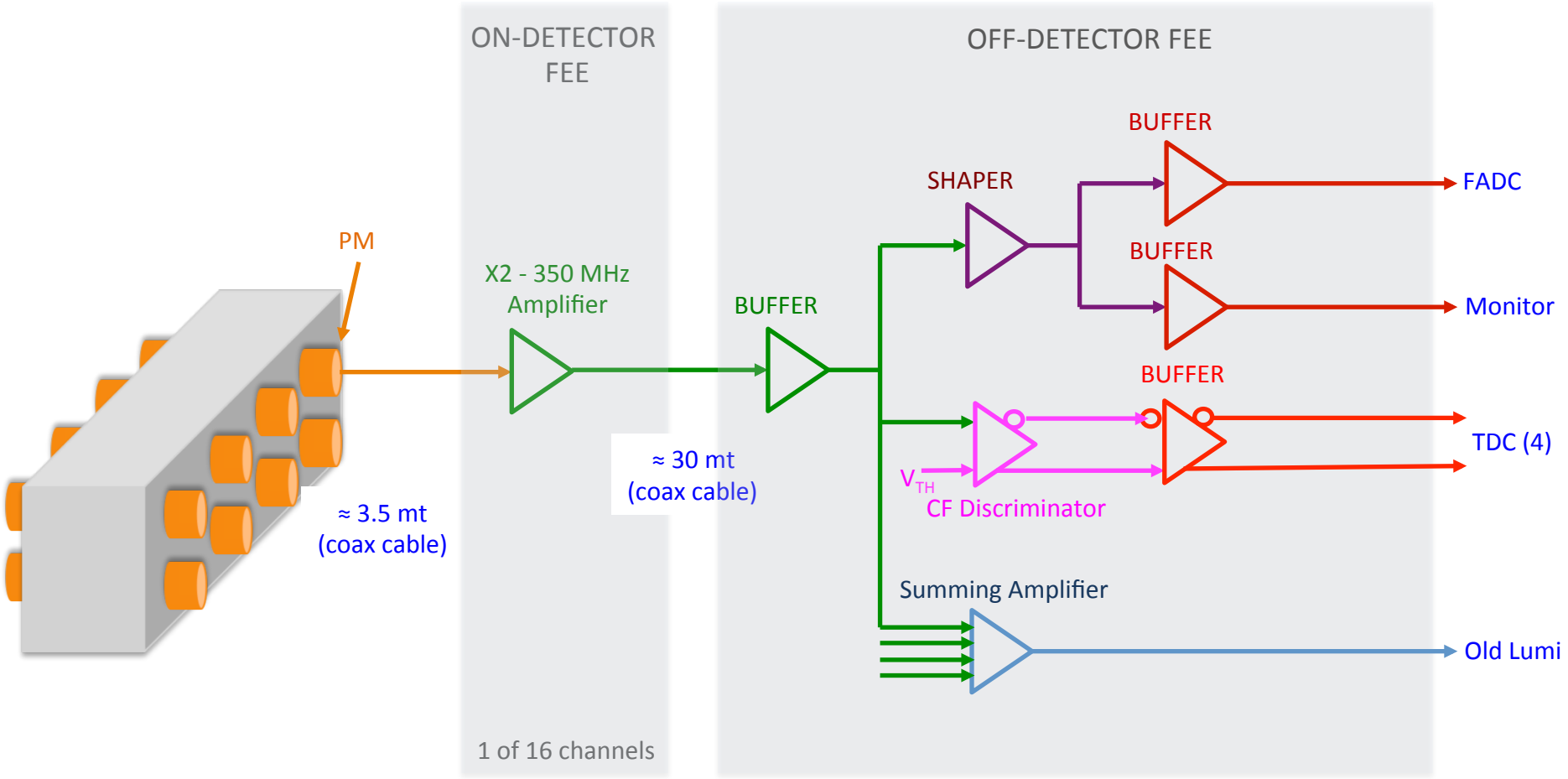
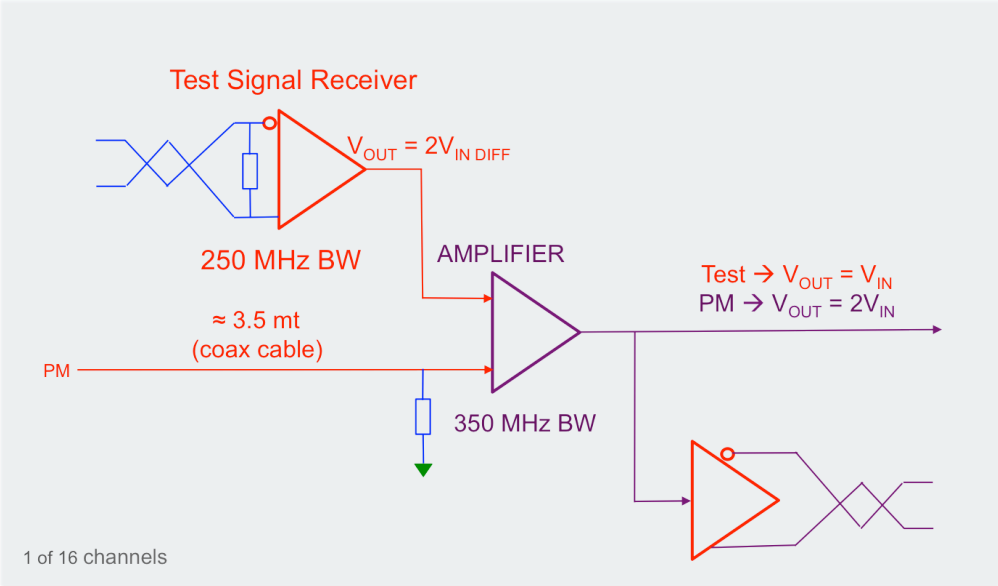
FEE Block Diagram

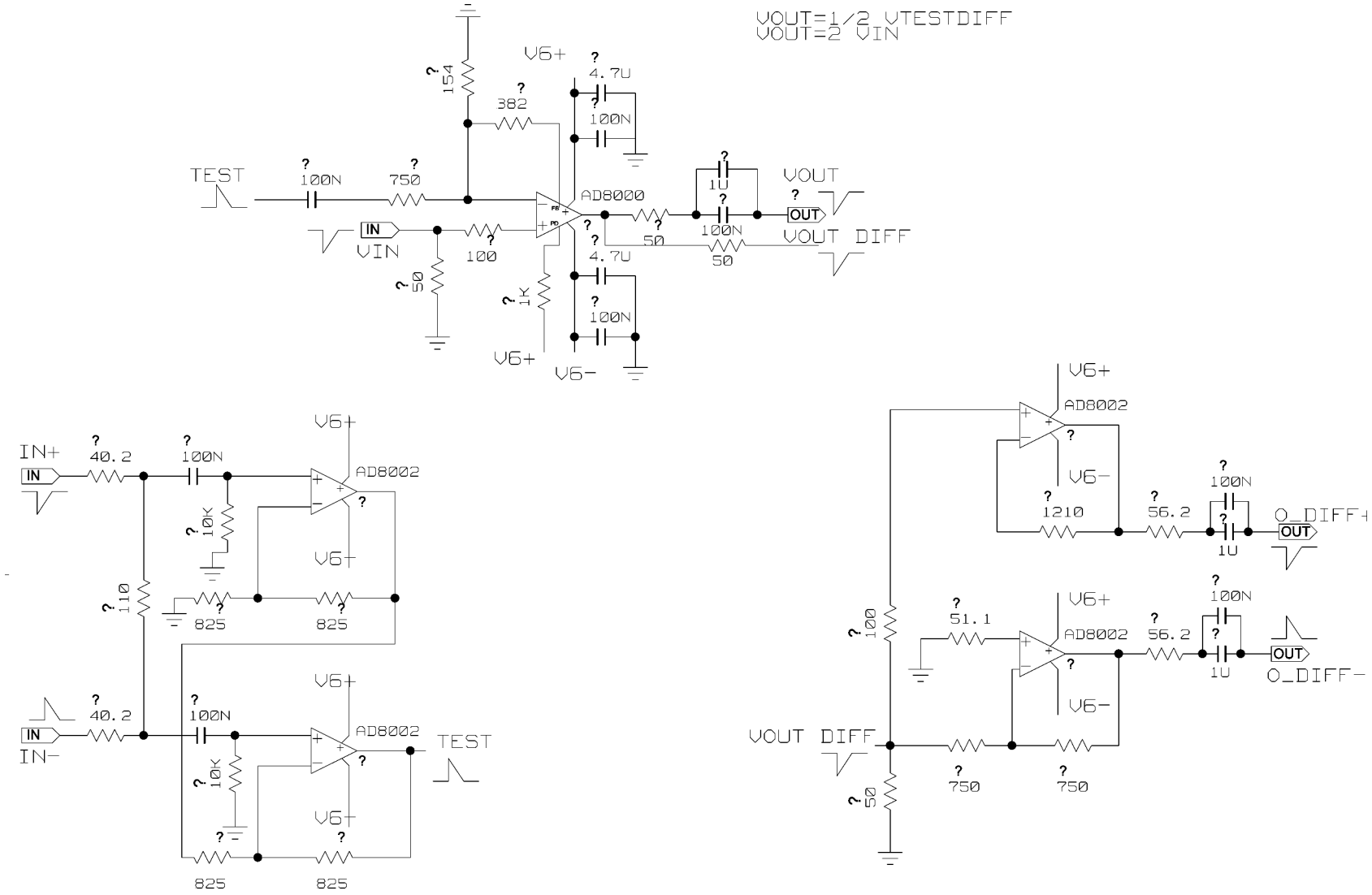


On-Detector FEE – Block Diagram & Requirements

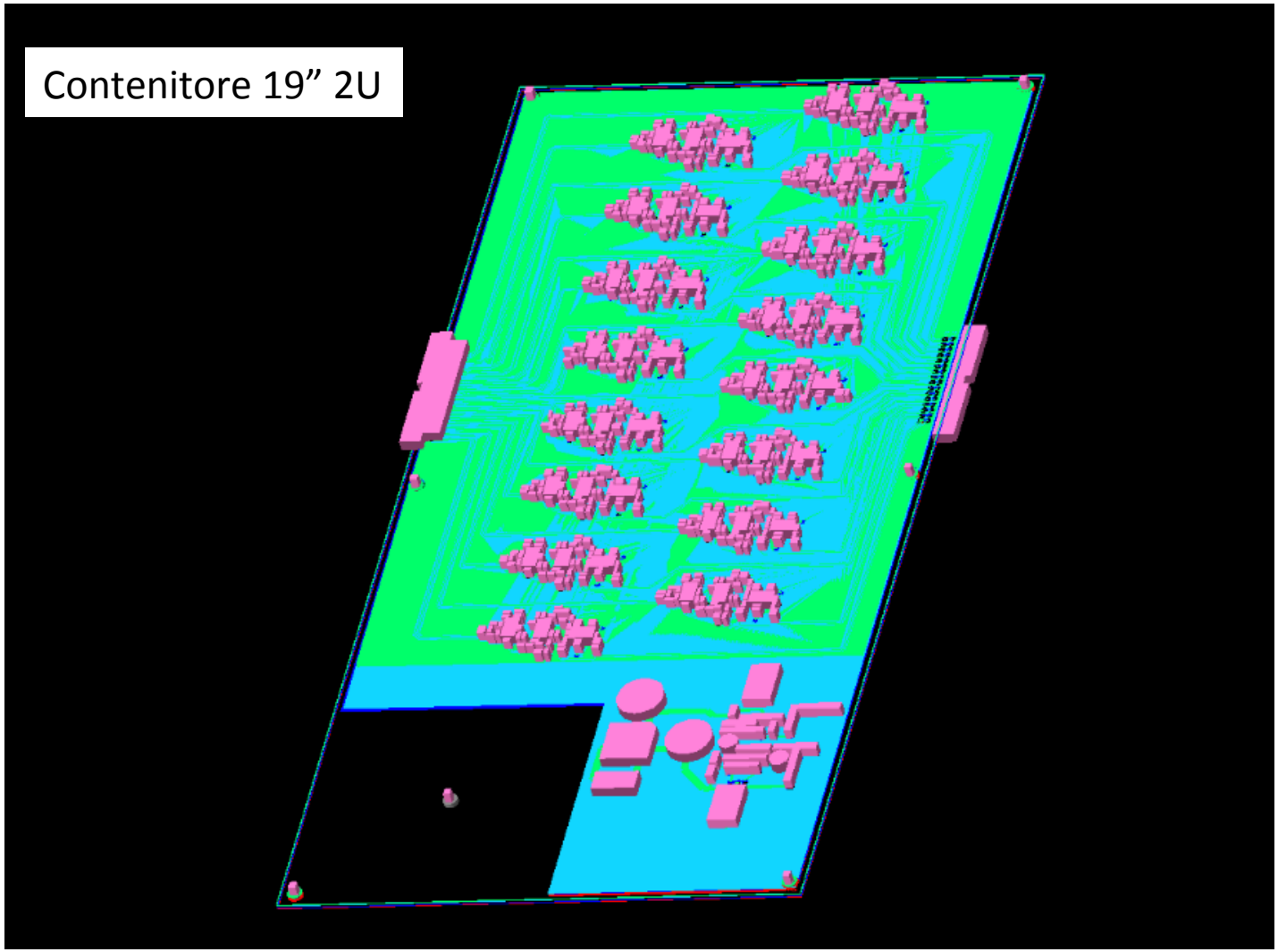
- 16 input signals from PM (40mV – 400 mV range - 1.5 ns rise time - negative polarity)
- ≈ 3 mt coax cable input connections - ≈ 30 mt coax cable output connections



On-Detector FEE - Schematics

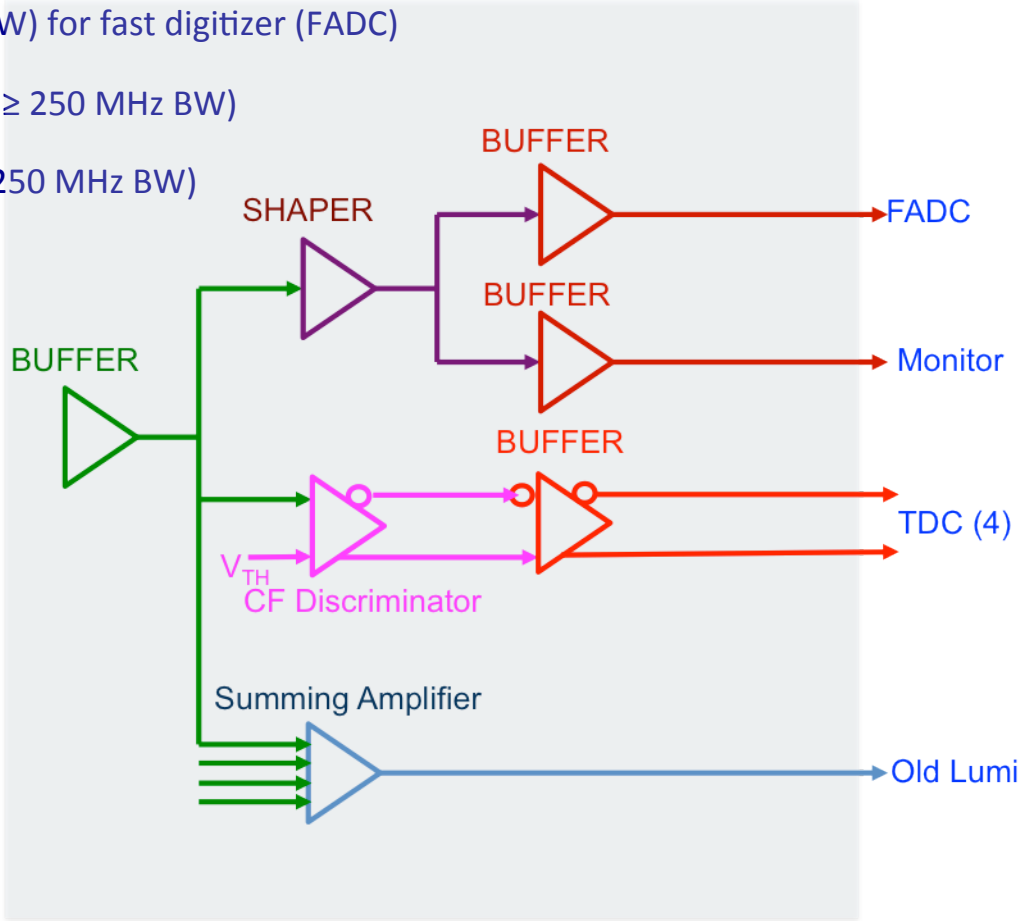


On-Detector FEE - Master

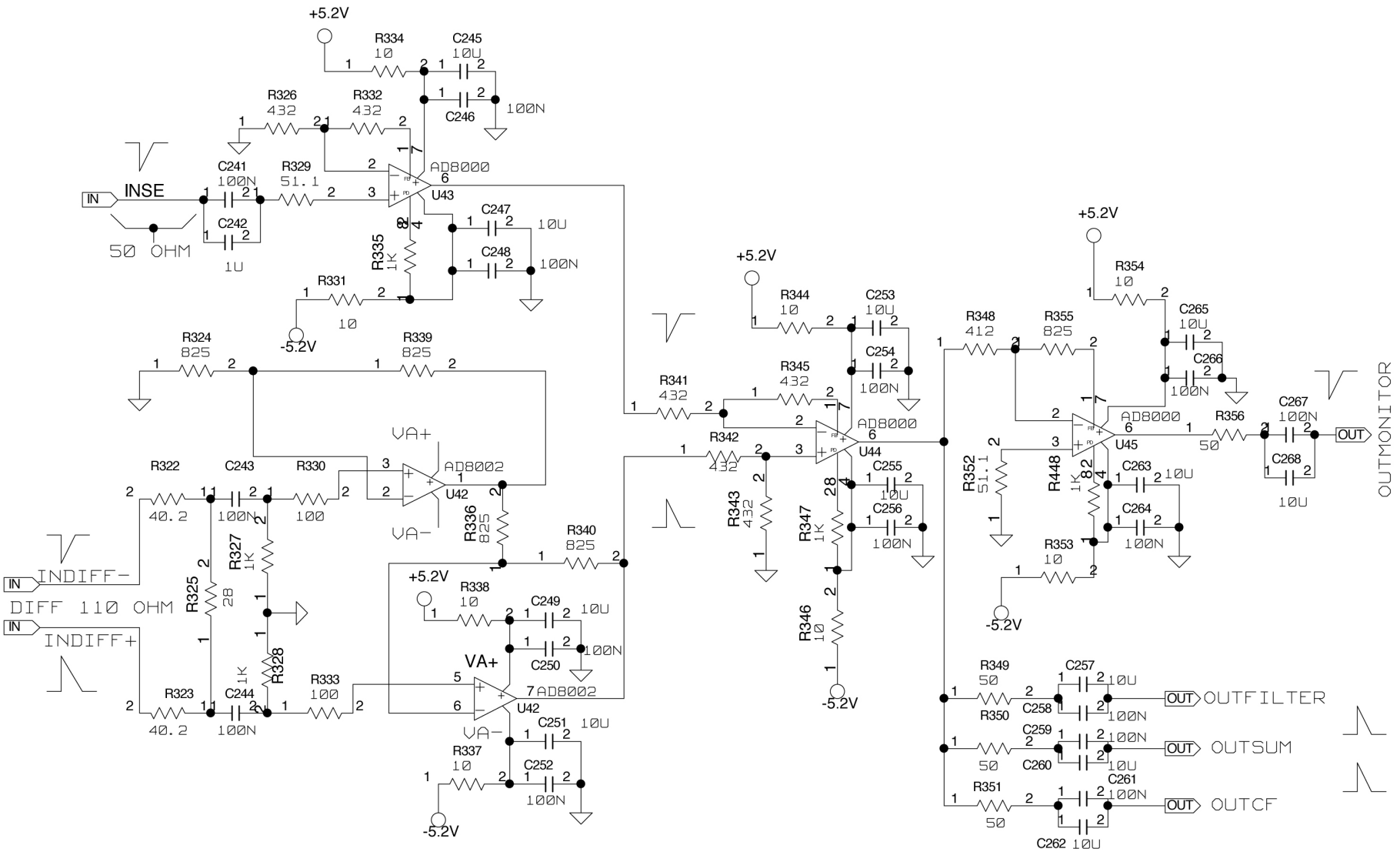


Off-Detector FEE – Block Diagram & Requiremnts

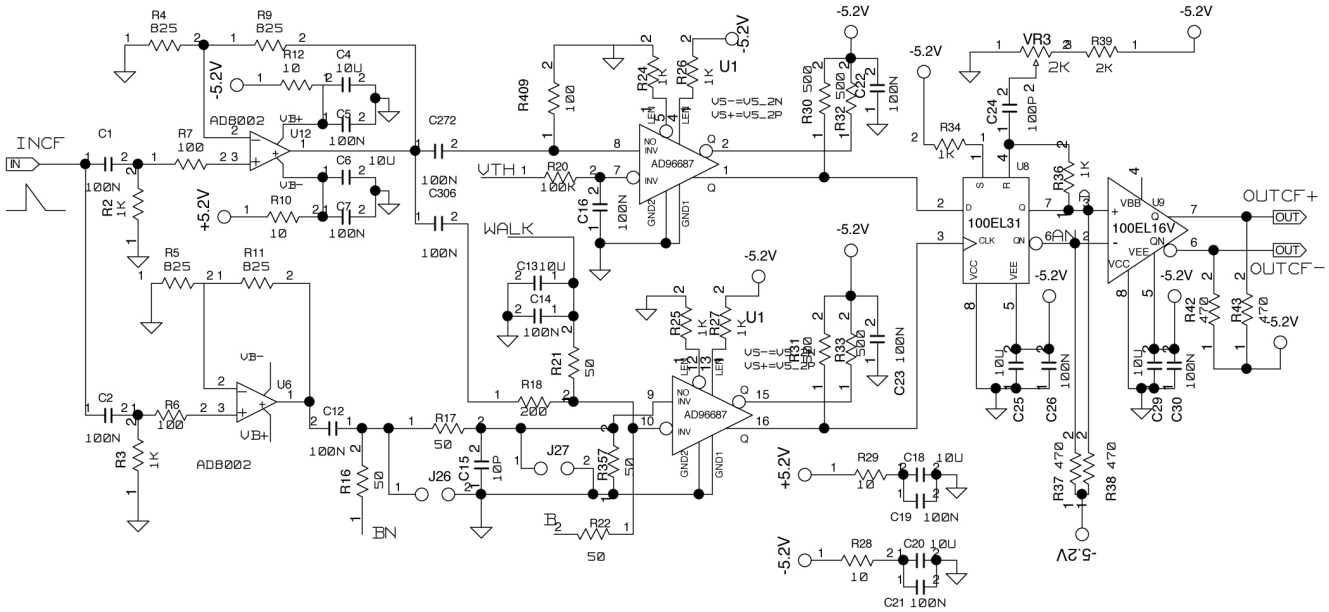
- 4 chs modularity
- Input signal : 80mV - 800 mV range - 1.5 ns rise time - negative polarity - 50 Ω
- Output signals :
  - Analog shaped output (≈ 125 MHz BW) for fast digitizer (FADC)
  - Analog output for monitor propose (≥ 250 MHz BW)
  - Analog sum output for Old Lumi (≥ 250 MHz BW)
  - Digital output for TDC

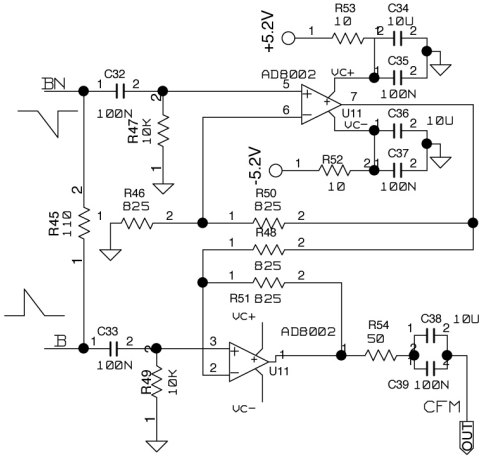


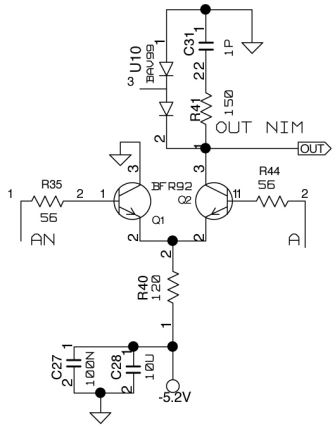
Off-Detector FEE - Receiver

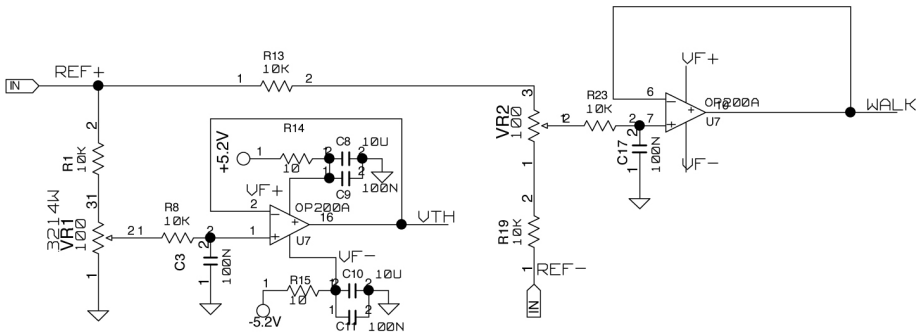


Off-Detector FEE – CF discriminator

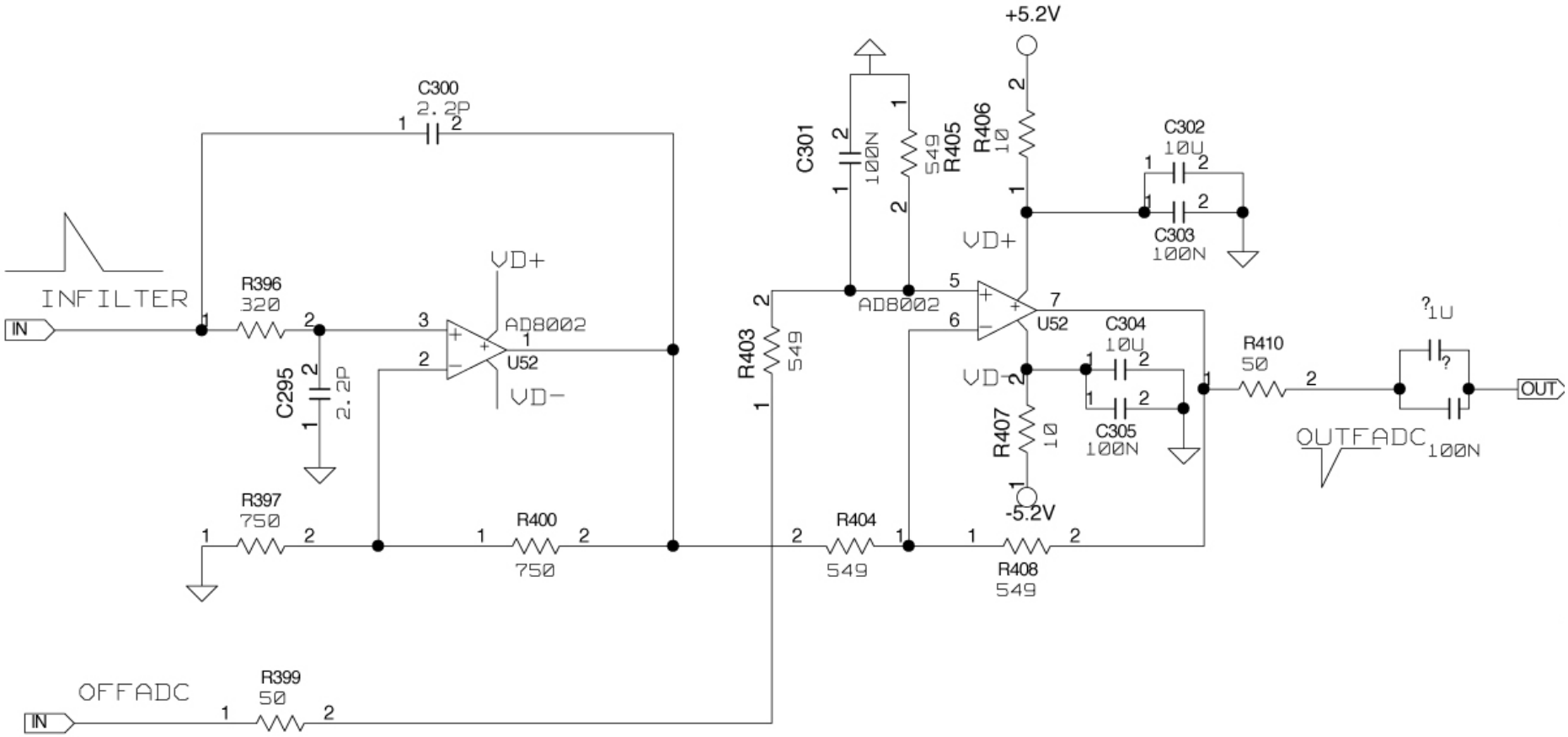




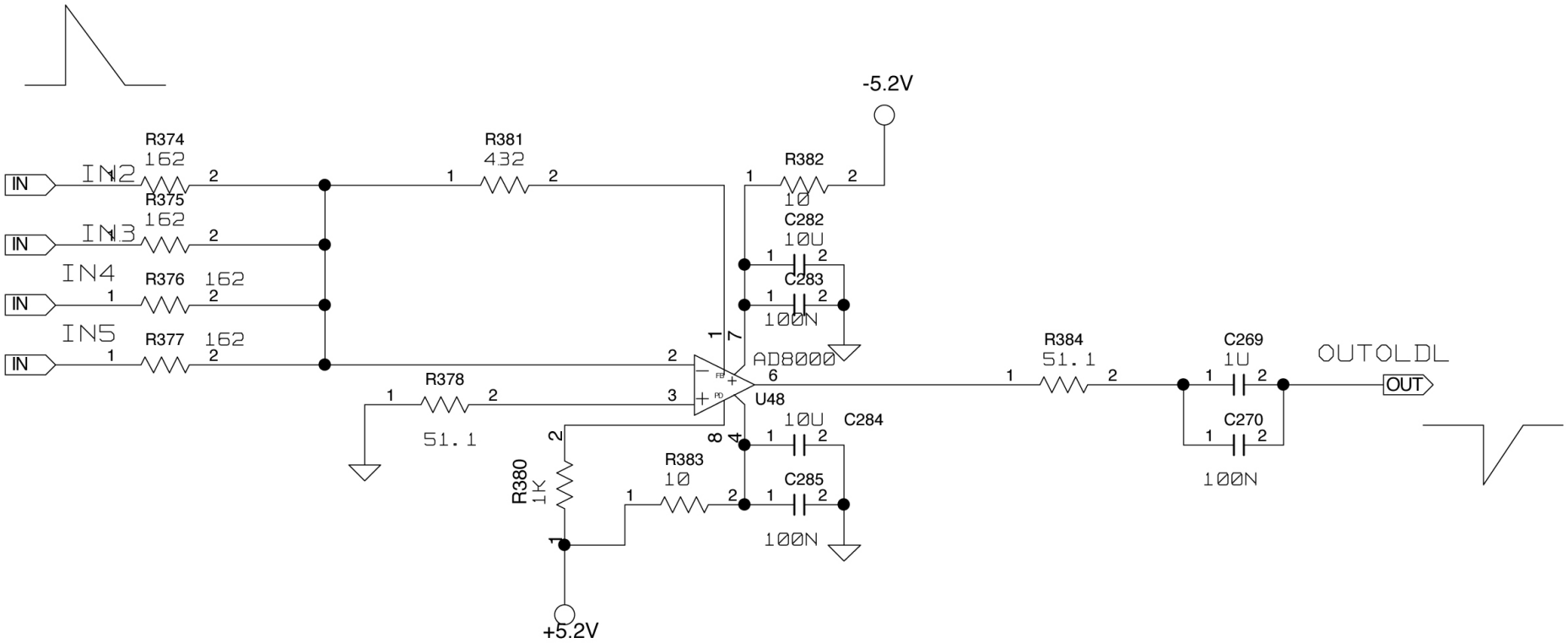




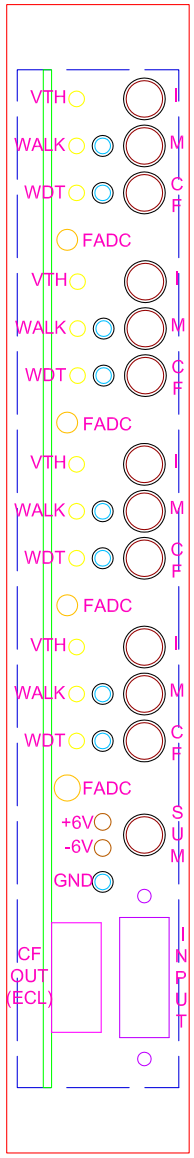
Off-Detector FEE – ADC anti-aliasing filter

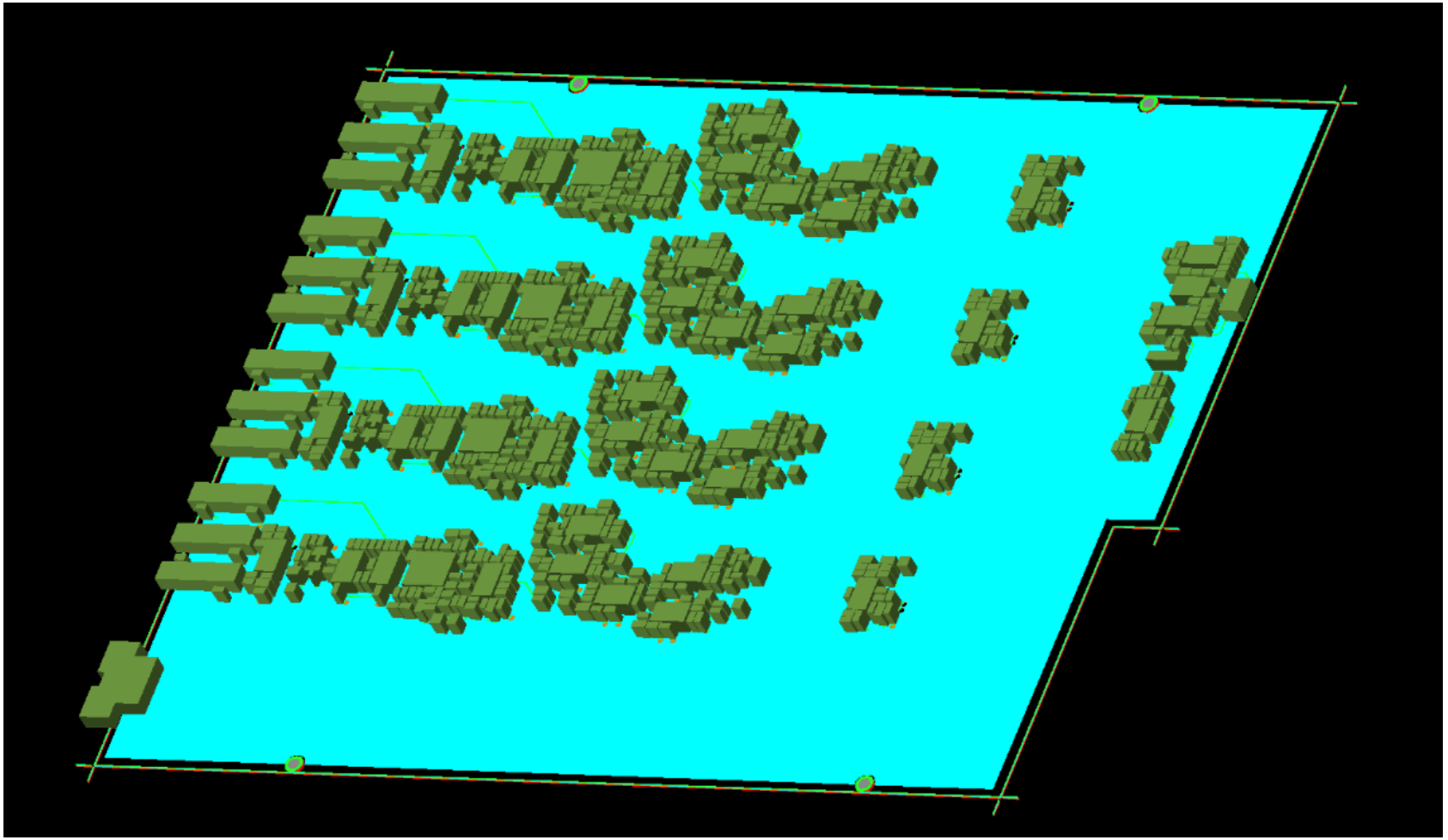


Off-Detector FEE – Summing Amplifier



Off-Detector FEE – Master





Front-End status

	ON-DETECTOR	OFF-DETECTOR	
PCB Layout	✔	25/3	
PCB Production	in corso	22/4	
Ordine Componenti	in corso	In corso	
Meccanica	✔	In corso	
Assemblaggio	8/4	29/4	
Test	18/4	6/5	

Goal : 1 modulo on-detector FE (16 chs) + 1 modulo off-detector (4 chs) entro il 15/5