Read-out of High Speed S-LINK Data Via a Buffered PCI Card

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Talk for the 4th PCaPAC International Workshop

- This is the paper copy version of the presentation-
Slide 9th is repeated due to an animation

CERN- EP division, ED Electronics group

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Contents

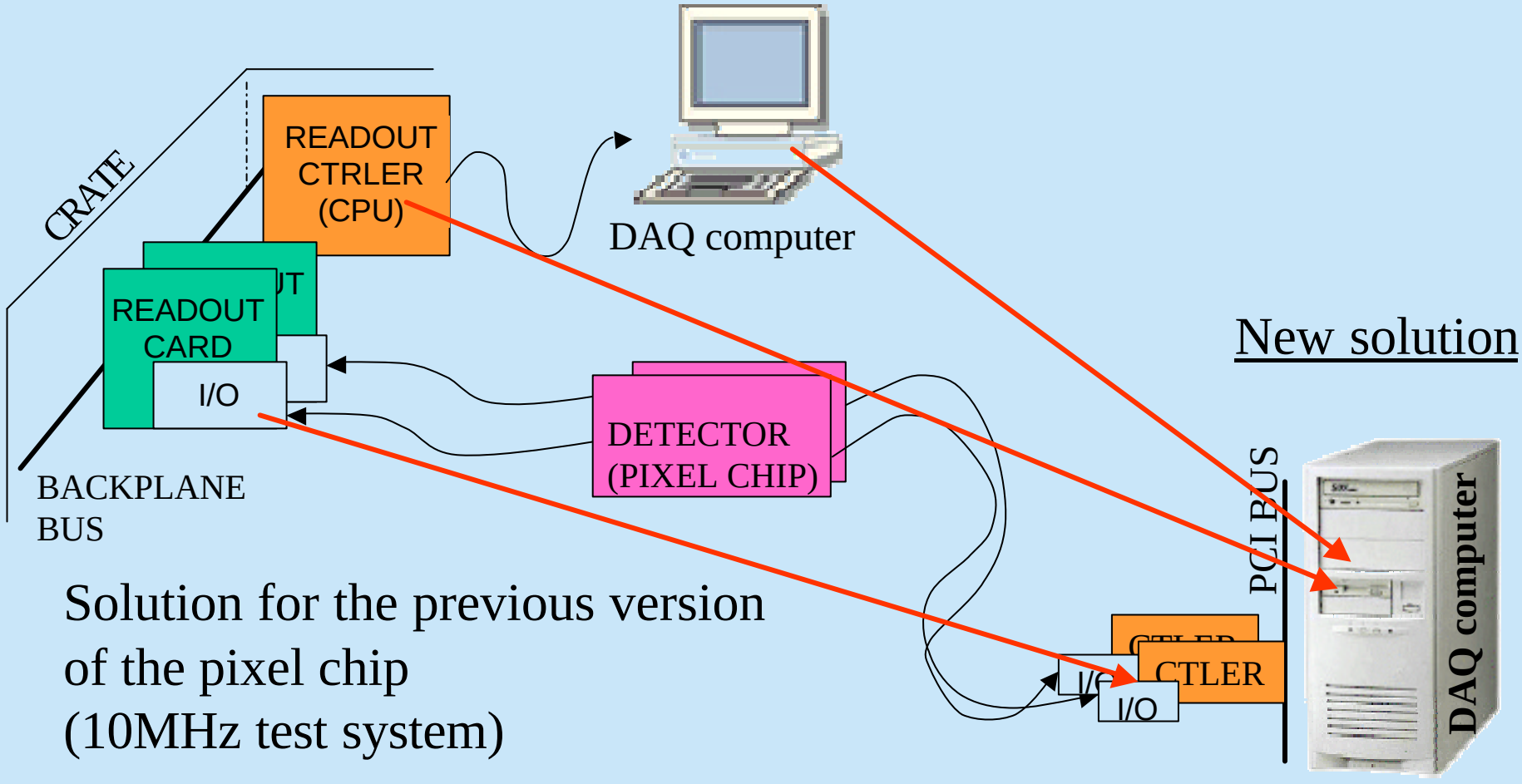
- Introduction to project requirements
- Minimizing a previous test system
- What the PC architecture and PCI offer
- The concept of the new solution
- Building the real system
- S-LINK Front-end electronics
- PCI hardware readout controller
- Software control interface
- Performance
- Conclusions and outlook

Project Requirements

Laboratory test system for LHCb RICH Pixel Chips

- **Test system on-line within 3 months**
- **40MHz clock rate**
- **1MHz event-rate, 32 DWORDs burst per event**
- **Inexpensive**
- **Flexible functionality**
- **Portable and handy– different applications**
  - **Chip characterisation**
  - **Wafer testing**
  - **Module (Photodetector) testing**
  - **Testbeams**

Minimizing a PIXEL chip test system



Solution for the previous version of the pixel chip (10MHz test system)

The PC architecture and PCI

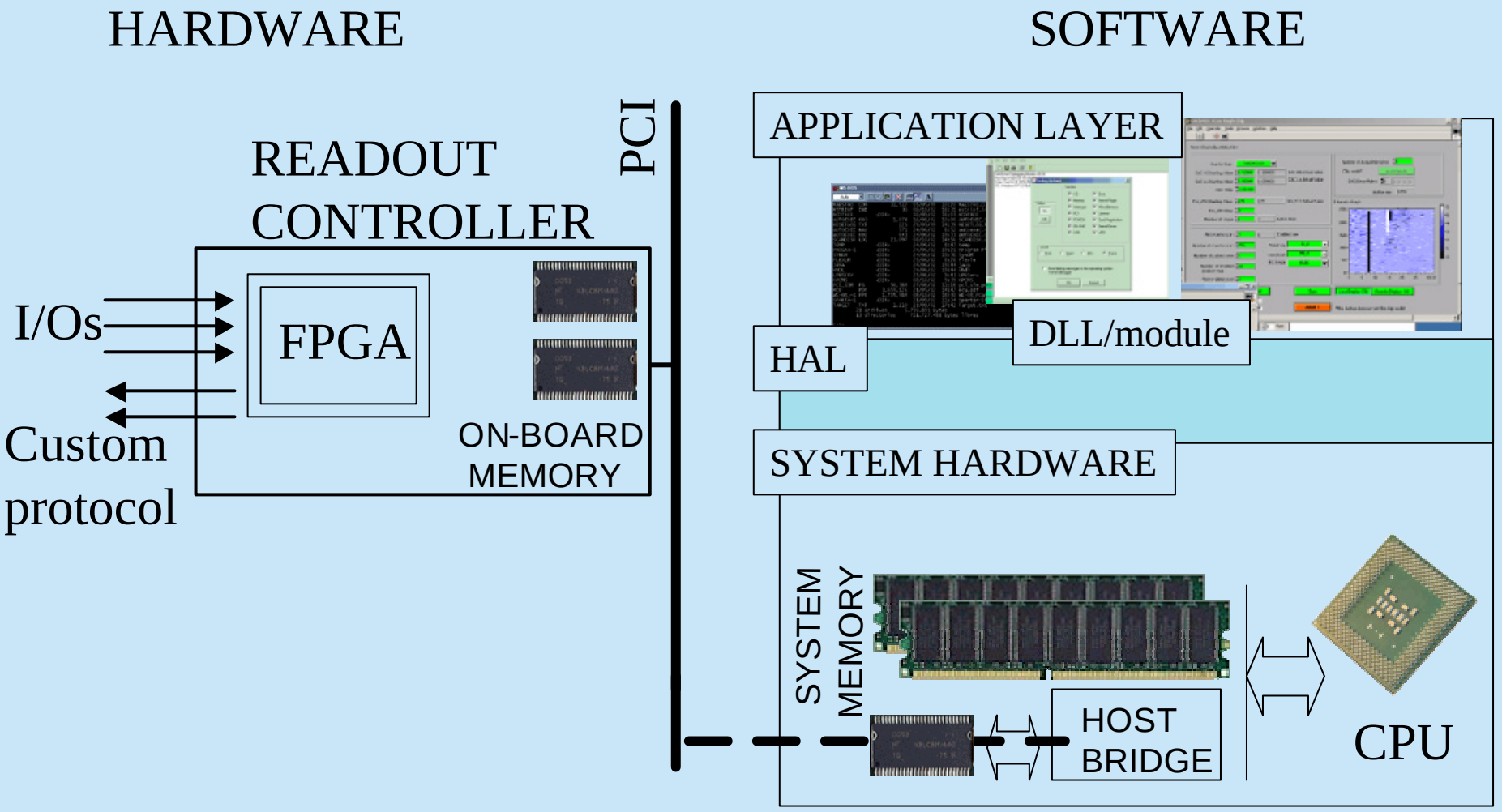
Advantages:

- **CPUs and many hardware resources available**
- **Most common and familiar bus architecture**
- **FPGA support**
- **Any conventional OS works with the PCI**
- **Low cost**
- **Partitionable (several controllers per bus)**
- **PCI 32b@33MHz, 64b@66MHz, cPCI available**

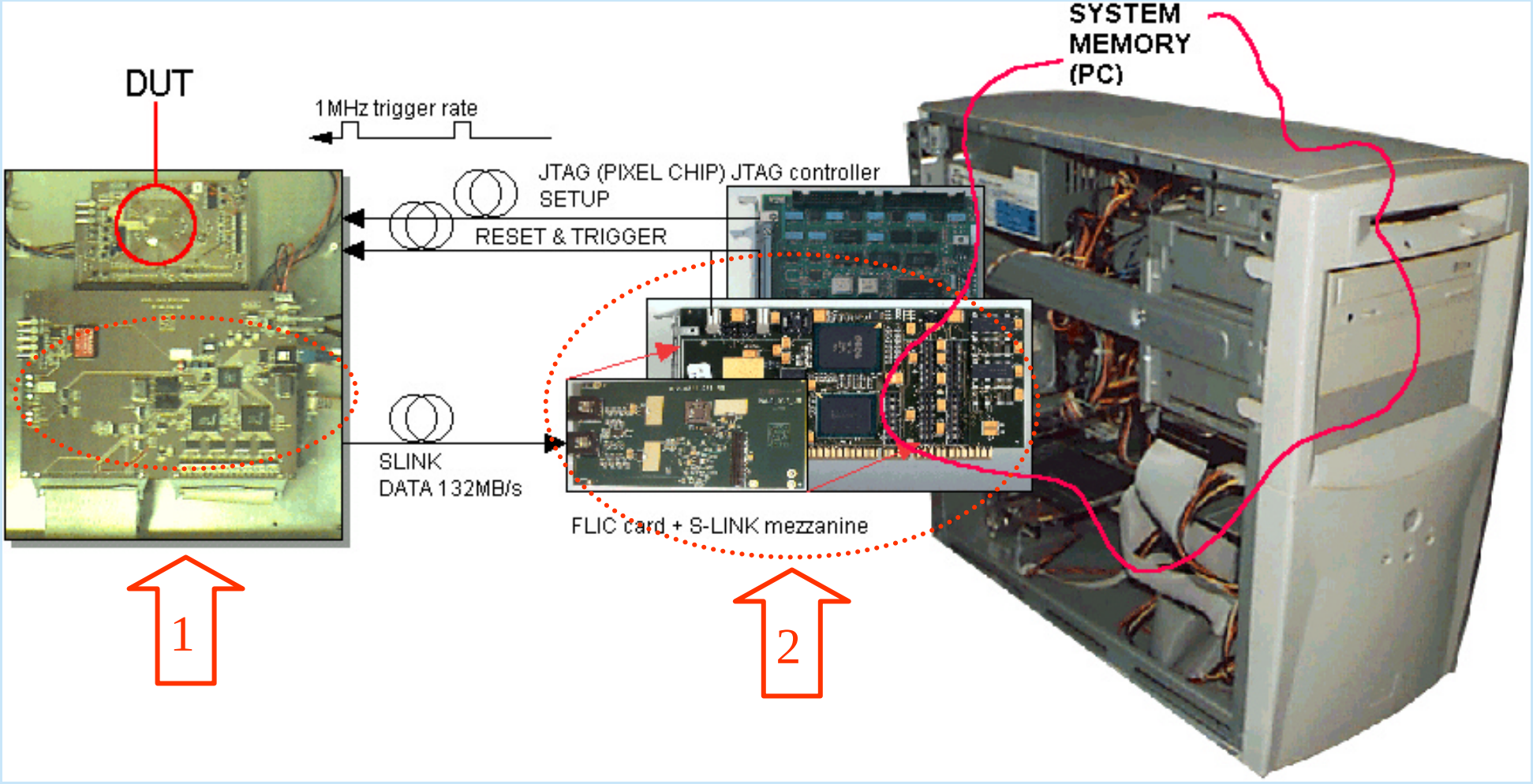
Drawbacks:

- **Limited space for electronics**
- **Limited power**

Concept of the new solution



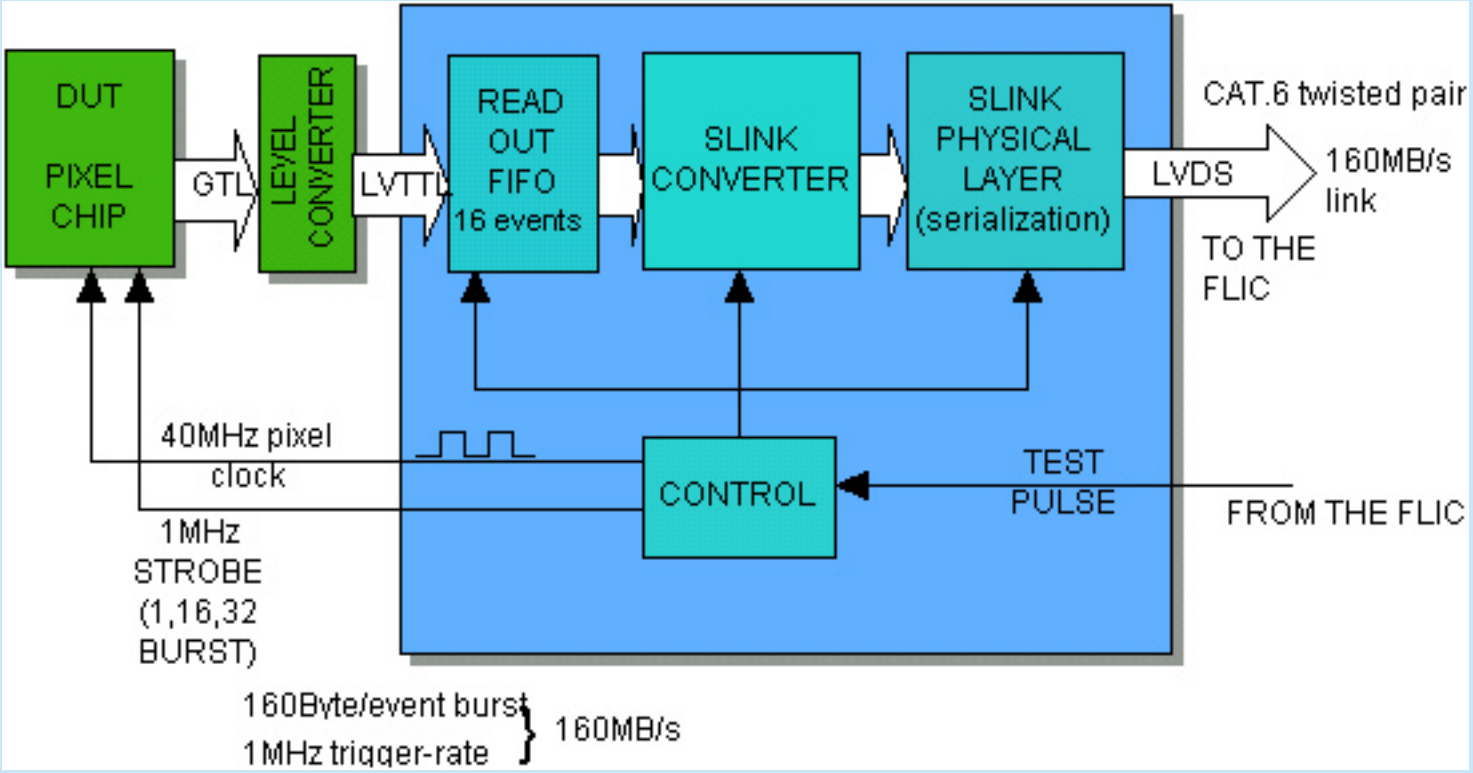
Building a real system



S-LINK Front-End electronics

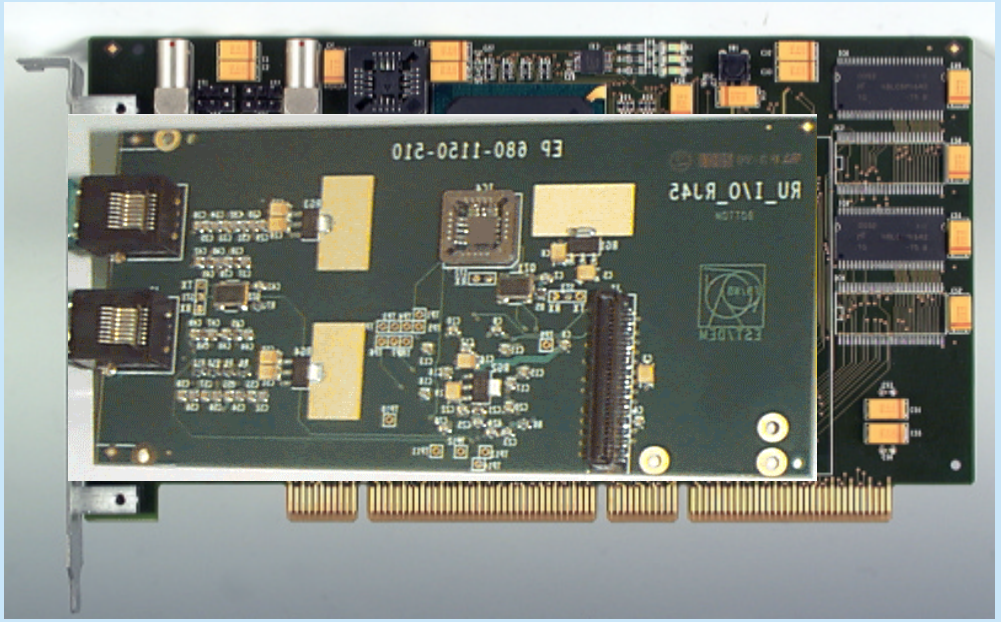
Single mode (32 dwords for LHCb) or multievent readout mode (up to 16 events per trigger)

Adaptation of S-LINK bus width for LVDS serializers



PCI Readout Controller

The FLIC card



- Standard PCI card
  - small, familiar
- Easy to use (Plug&Play)
- General Purpose solution
  - Mezzanine cards interchangeable
  - Custom HW interface (FPGA, HDL)
- Low cost
- Large data buffer → local memory becomes system memory

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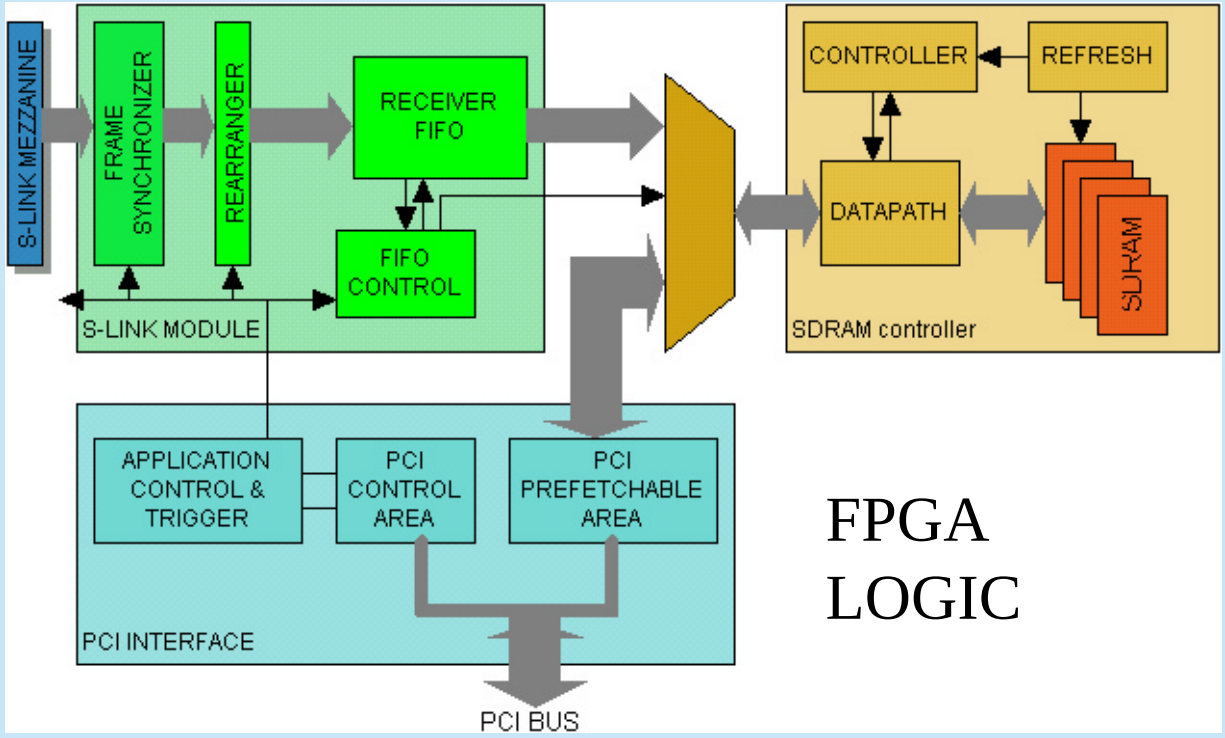
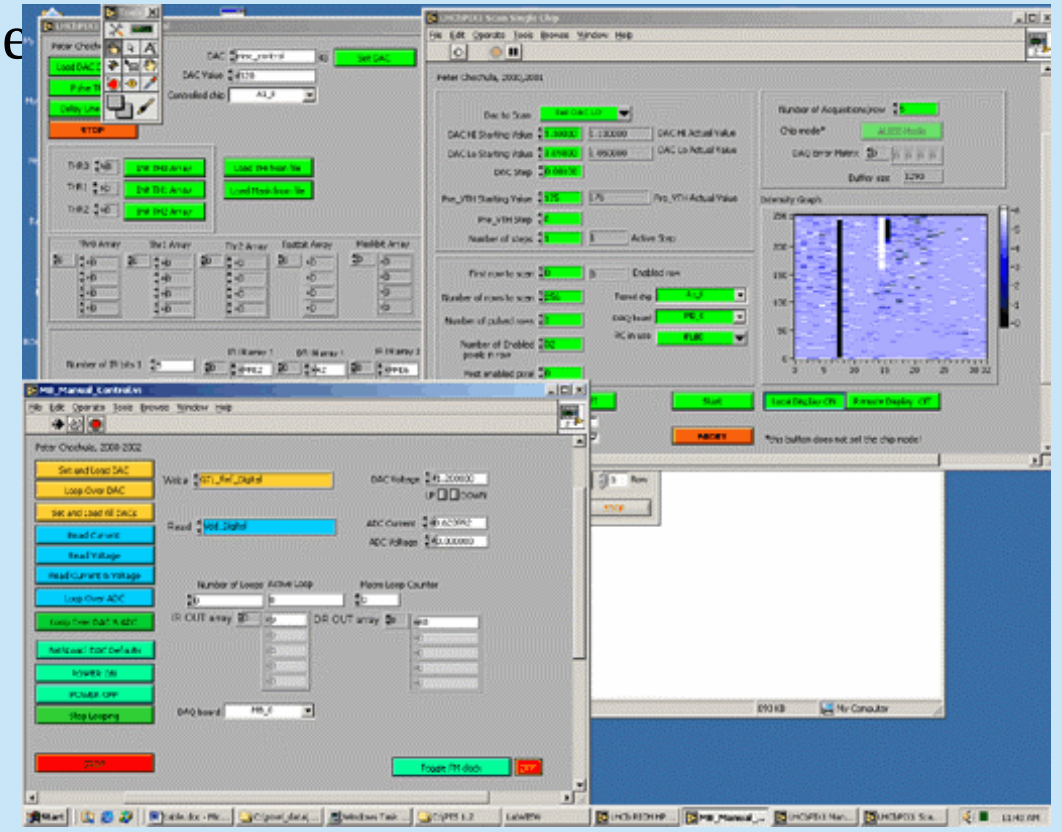
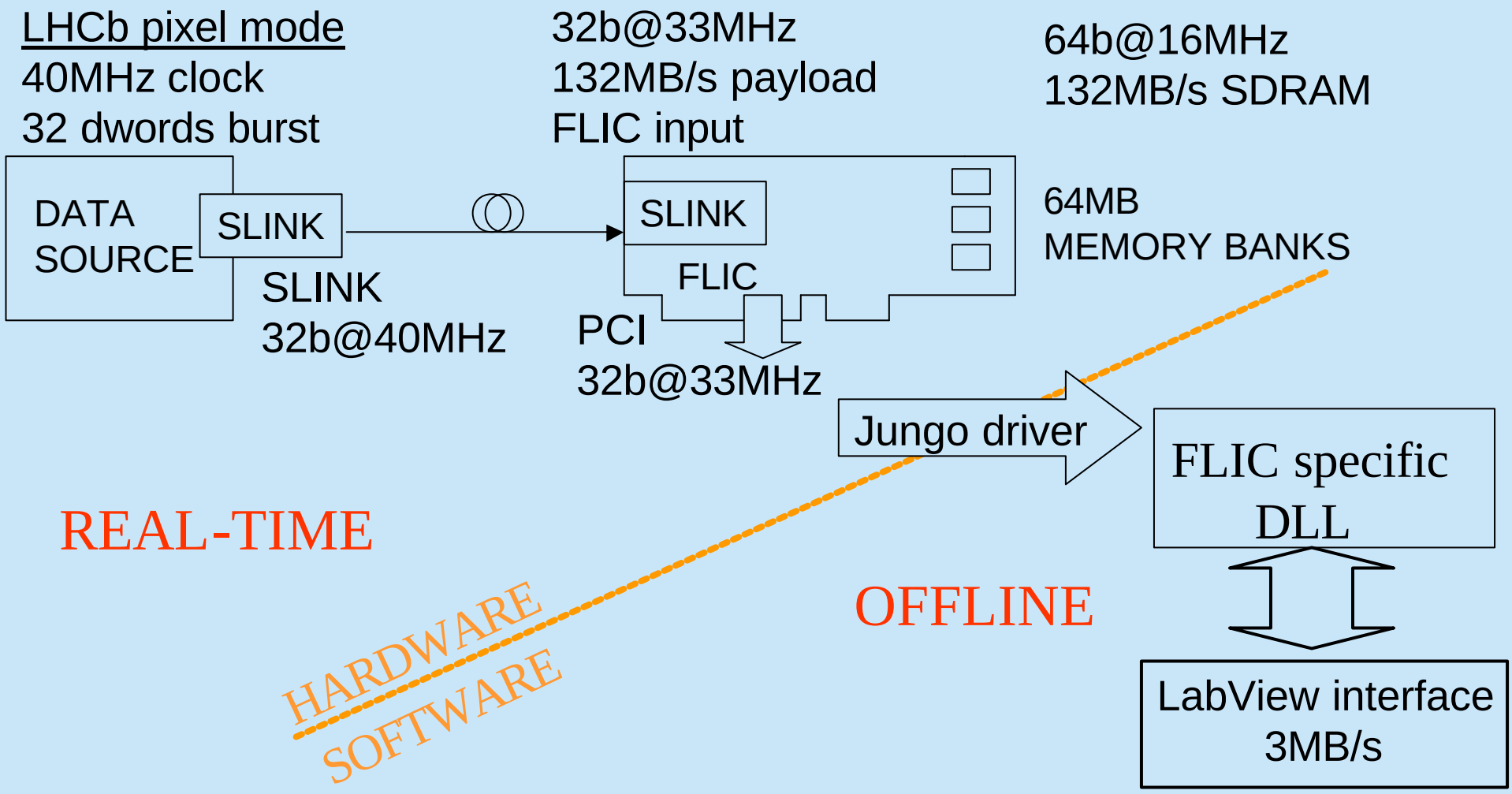


Readout Software

- LabView Analysis and Interface
  - ✍Existing analysis software for the chip
  - ✍Interface with commercial cards (JTAG controller)
- Need of developing a Windows™ driver for the FLIC
- Existing support for Linux



Performance



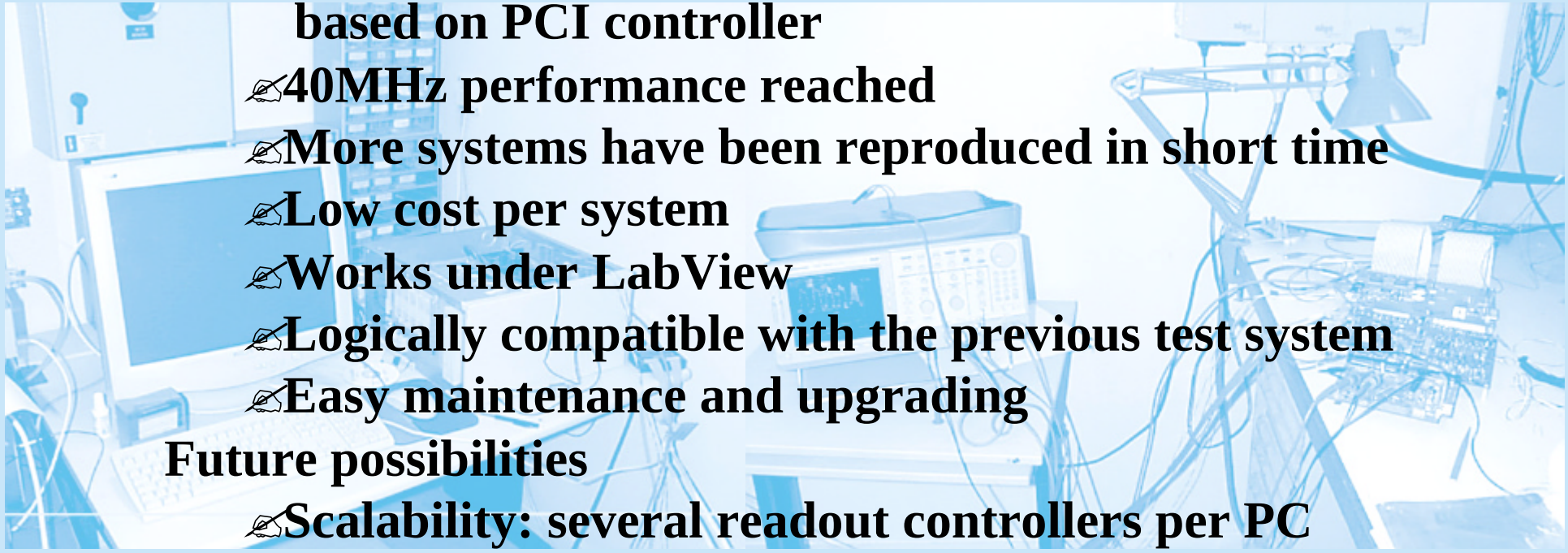
Conclusions and Future

Conclusions

- **A test system has been built based on PCI controller**
- **40MHz performance reached**
- **More systems have been reproduced in short time**
- **Low cost per system**
- **Works under LabView**
- **Logically compatible with the previous test system**
- **Easy maintenance and upgrading**

Future possibilities

- **Scalability: several readout controllers per PC**
- **Higher speed in the software domain (DMA engines)**
- **More complex controllers may fit in larger FPGAs**



Thanks!