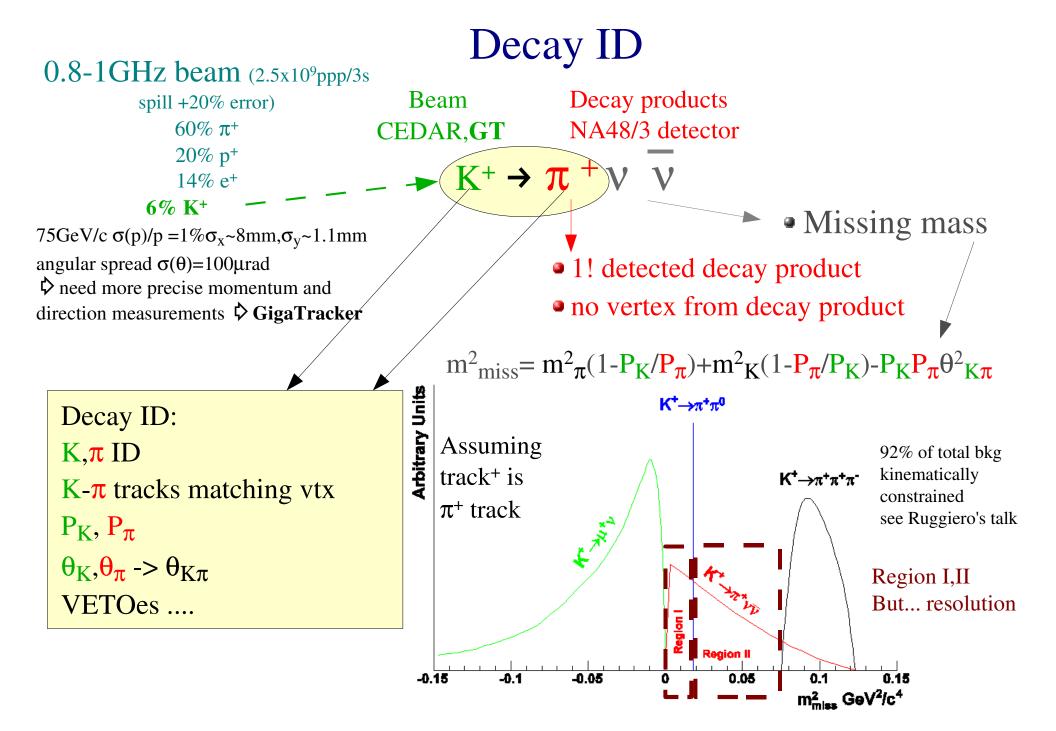
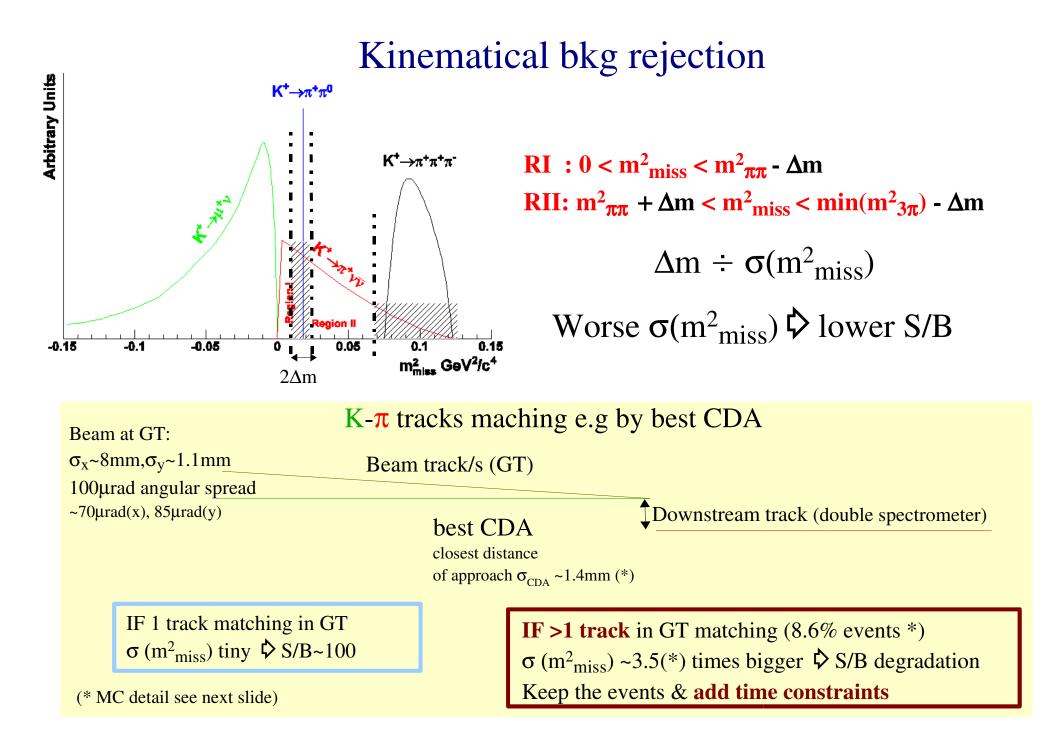
# The NA48/3 GigaTracker

## Alias Tracking in the beam at 1GHz rate

- GigaTracker: Decay ID & bkg rejection
- Requirements
- In the beam
- Resolution & material budget
- Rate & dose
- Time resolution

K Rare decays meeting, Frascati 26-27.05.2005 M. Scarpa INFN and University of Ferrara





### Requirements on GT from

The experiment:

• Acceptance 10% (50% data taking efficiency included)

● S/B≥10



- Beam K<sup>+</sup> 75GeV/c momentum bite 1%
- @GT  $\sigma_x \sim 8mm, \sigma_y \sim 1.1mm$
- minimum amount of material on beam X/X0<<1%</p>
- Tracking in a not uniform (converging beam) rate distribution
- total rate of ~1GHz out of which only ~6% are  $K^+$
- High radiation level

The MC study on  $\pi^+\pi^0$ 

assuming

• photon rejection inefficiency 2x10<sup>-8</sup>

•  $(15 < P_{\pi} < 35)GeV/c$ 

• Hodoscope event time  $\sigma(t) \sim 50$  ps

• Double spectrometer: straws ~0.5%X0 per chamber,

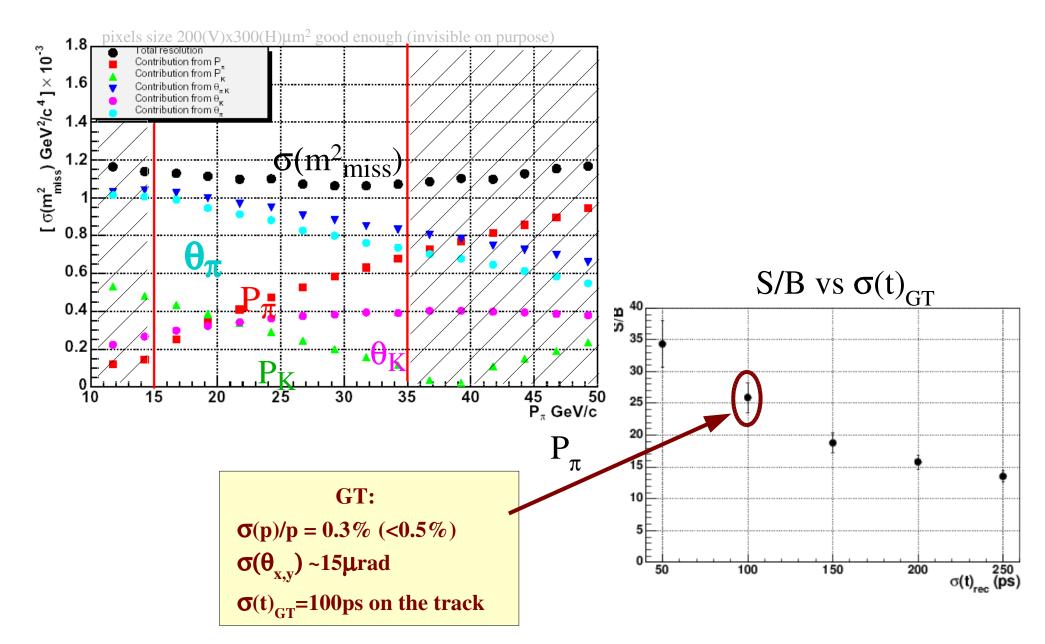
spatial resolution 120µm per view 100% reconstruction efficiency,

**Double spectrometer**  $\sigma(p)/p = 0.33\% \oplus 0.0077\% p$ ,  $\sigma(\theta)$  in X and Y projections ~30µrad not spoil the spectrometer angular measurements: minimize MS in the last part of GT

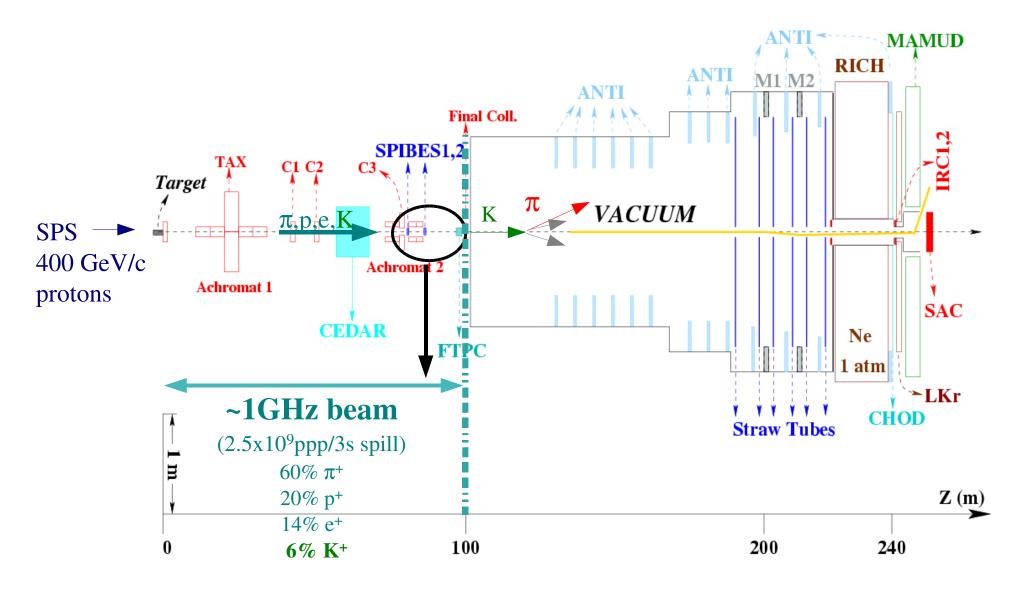
with **GT:**  $\sigma(\mathbf{p})/\mathbf{p} = 0.3\%$ ,  $\sigma(\theta)$  in X and Y projections ~15µrad  $\diamond$  ~8.6% events have >1 track matching in GT with bestCDA(\*) approach, reducible to ~3% by time coincidence in  $\pm 2\sigma(t)_{GT}$  **IF**  $\sigma(t)_{GT} = 100 \text{ps}$   $\diamond$  S/B ~25

(\*) might be improved by other matching methods e.g. 2D impact parameter

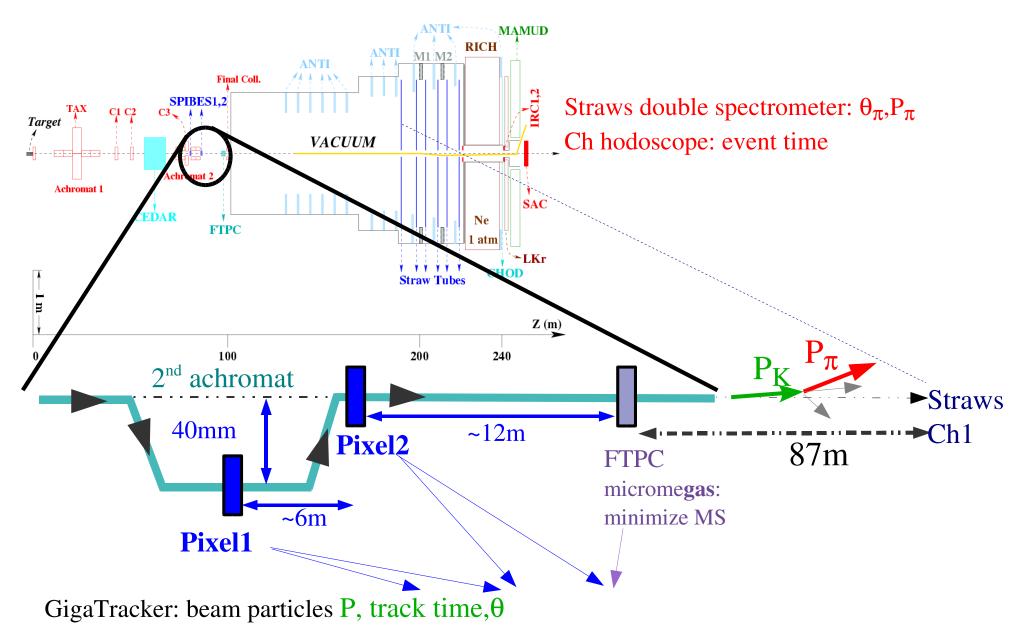
### MC Requirements on GT



### In the beam....



### In the beam with GT



### Resolution and material budget

#### Station 1 and 2: hybrid Silicon pixels

- Minimize material on beam
- produce signals, fast signals
- electronics
- cooling
- support
- respecting the NA48/3 requirements and timescale

### $\mathbf{\nabla}$

Hybrid Silicon (X<sub>0</sub>=9.36cm) pixel detectors: Silicon sensor bump bonded (~0.01%X<sub>0</sub>) to Silicon chip

beam

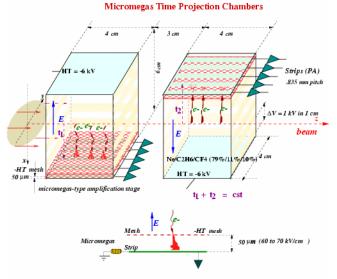
- cooling & support with the same CFiber
- ➢ In vacuum (save 100µm mylar windows front and back: 0.7%X<sub>0</sub>) → cooling by conduction

Station 3: FlashTPC

Minimize MS effect on downstream detector measurements (especially angle)

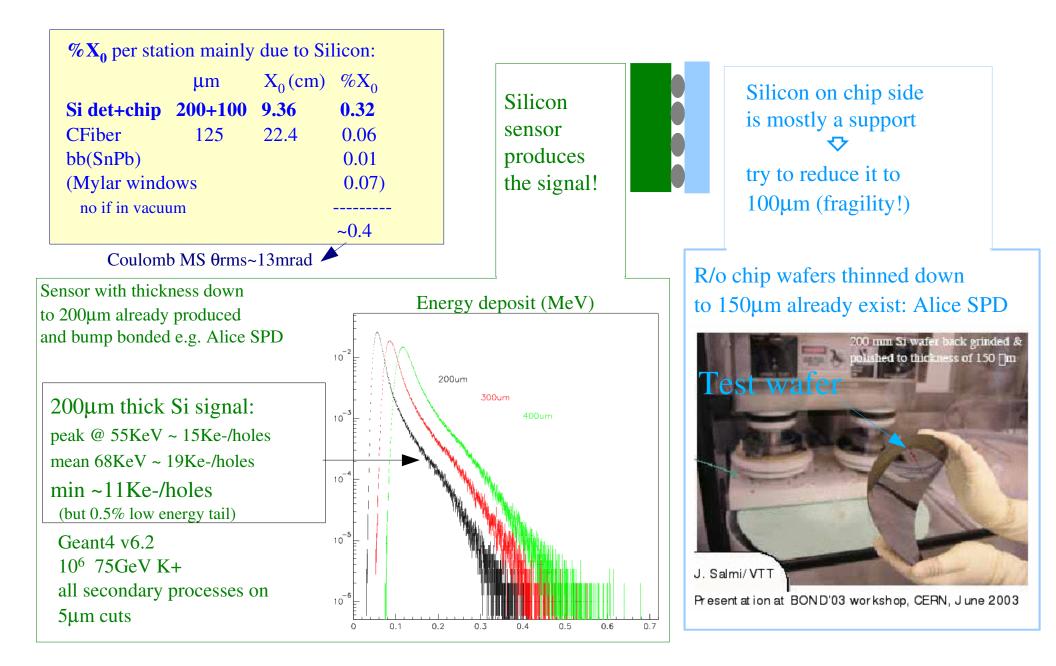
TPC with micromegas amplificationUpgraded version of Kabes-NA48/2:Position resolution 80μm

- $\circ \sigma_t = 0.7 ns$
- max strip rate ~2MHz

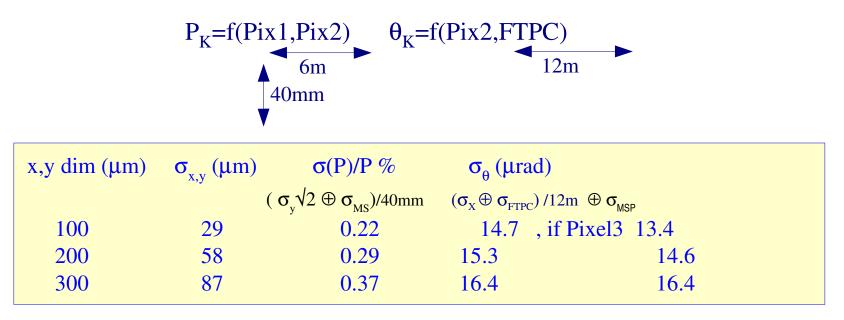


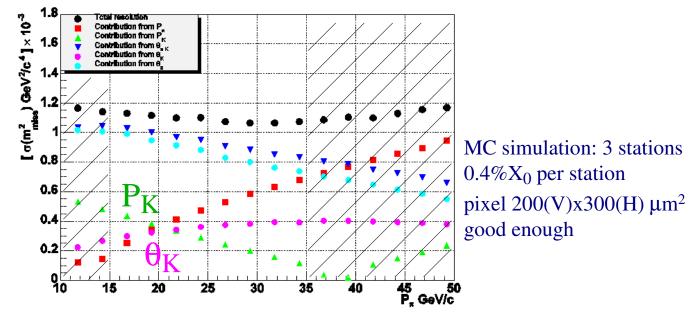
Reduce the amplification gap, sampling each strip with 1GHz FADC, sustain 10x higher rate per unit area

### Pixel stations material budget



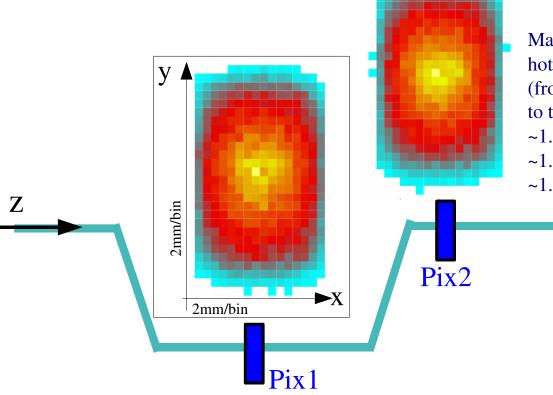
## Pixel size and resolutions



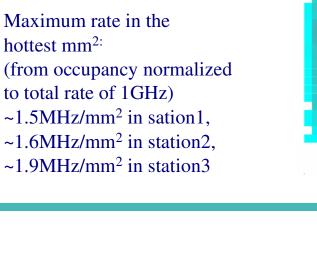


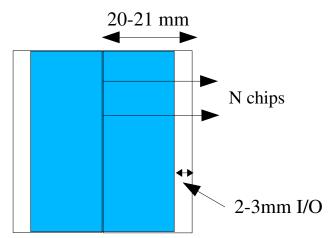
## **Rate and radiation at GigaTracker I**

Average rate per station ~60MHz/cm<sup>2</sup> Converging beam: rate not uniform, higher rate in the center



GT area per pixel station (beam tails<10<sup>-4</sup>): 36mm(X) x 48mm(Y) but Photolithographic process for r/o chip max 20-21mm wide 2 half detectors to cover the area

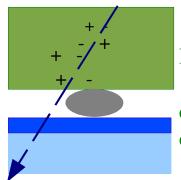




**FTPC** 

## **Rate and radiation at GigaTracker II**

#### Radiation damage on pixels detector



CMOS readout chip: sensitive components close to the surface

 Total Ionizing Dose (TID) ionization in SiO<sub>2</sub> layer and defects creation SiO<sub>2</sub>-Si interface

#### ዏ

- transistor level leakage (mainly digital)

enclosed transistors

- threshold voltage shift (analogue)

 sub-micron tech e.g. 0.25μm or 0.13μm (the thinner the oxide the best)

• Single Event Upset (SEU) (reversible) affecting bit

redundancy e.g. cells x3 & major voting or special coding schemes Sensor: full bulk sensitive to damage Bulk damage

change electrical characteristics, evolves with time and doesn't stop when stopping irradiation

Increase I<sub>leak</sub> ÷ exp(-Egap/2KT) due to generation/recombination levels
 Cooling, thinner sensor, sensor technology and design

• Change in V<sub>d</sub> (depletion voltage):

#### type 'inversion': n-type bulk behave like

**p-type**, depletion from backside and  $V_d$  increase with fluence, risk to operate with under-depleted sensor: charge loss and spread. Too high voltages --> current break down

#### Annealing effect (beneficial and reverse) long term exposition , temperature dependent

## **Rate and radiation at GigaTracker III**

Per GT station in NA48/3 beam the expected average particle flux/cm<sup>2</sup> per day is:

1GHz\*3.125s(eff spill)\*5000(spills/day)/area ~ 9x10<sup>12</sup> particles/cm<sup>2</sup>day

• Approx  $\pi$  only beam (60%)

• conversion factor 0.37 ratio of displacement damage cross sections for high energy (>GeV)  $\pi$ (35MeV mb) and 1MeV neutron (95MeV mb) (Huhtinen private communication, NIMA491)

• safety factor 2

 $\Phi_{eq}(1 \text{MeV n})/\text{cm}^2$  ~7x10<sup>11</sup> day ¢ 1MeV equiv n/cm<sup>2</sup>: norm fluence unit used to compare real beam with 1MeV n beam producing the same 7x10<sup>13</sup> **100 days** displacement damage x3 in the hottest mm<sup>2</sup> **Replace the**  $3x10^{14}$  CMS innermost pixels in 1 year pixel stations 3x10<sup>12</sup> ALICE pixels in 10 years every 2 weeks (profiting of SPS MD) 1-fewx10<sup>12</sup> expected n-type-inversion point

 $\Diamond$  easy replacement and alignment

and an average TID (rad) ~2Mrad in 100 days (2 yrs data taking)

R/O chip: up to TID=30Mrad with radiation tolerant layout (vast majority LHC experiment):

 $0.25\mu m CMOS + enclosed + guard rings$ 

(IEEE Vol.46 No.6 1999, G.Anelli Ph.D Thesis http://rd49.web.cern.ch/RD49/RD49Docs/anelli/these.html)

## **Time resolution requirement I**

- Requirement on spatial resolutions: easy with Si pixels + FTPC
- Requirement on material budget: easy FTPC, pixels less easy but feasible
- investigation on chip silicon thickness
- investigation on CF support and cooling (depends on chip consumption)

#### • Requirements on time resolution: 100ps on the track

#### ~150ps per pixel station(TDC)

high complexity R/O CHIP bump bonded on sensor

- on beam (radiation hardness technology --> space)
- analogue AND digital high frequency part together:

#### influence of the noisy digital part on the analogue part

Switching noise originated from the digital circuits can be coupled in the analog part through power and ground lines, parasitic capacitances between interconnection lines and, the most difficult to eliminate,common substrate noise

Building blocks: fast preamplifier and shaper,

low time walk discriminator,

high resolution TDC,

peripheral circuitry

- power dissipation

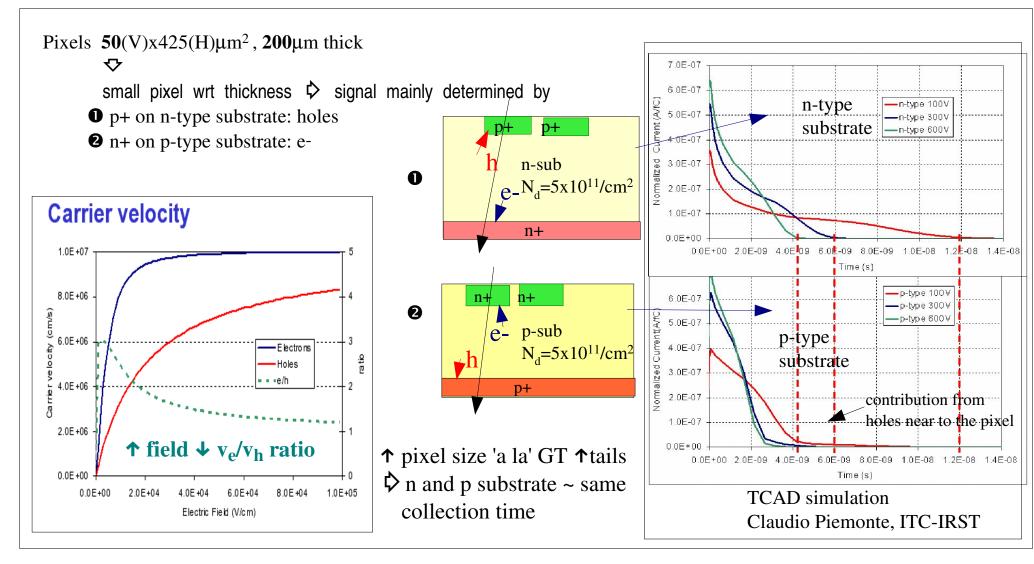
- technology CMOS process: 250nm might be insufficient  $\diamondsuit$  130nm

### **Time resolution requirement II**

Very challenging but good hints from TCAD simulations of 200µm thick sensor:

few ns charge collection time achievable using n or p substrates

Simulation on 'a la' ALICE pixels:  $50(V)x425(H)\mu m^2$ 



### Conclusions

#### GigaTracker: 2 pixels stations + 1FTPC for tracking @1GHz rate IN THE BEAM with excellent spatial (good if 200(V)x300(H) $\mu$ m<sup>2</sup> pixel and $\sigma$ = 80 $\mu$ m FTPC) AND time resolutions (100ps on the track \$\$\$\$ 150ps per TDC)

#### **FTPC upgrade**

#### **New Pixel stations**

- sensor (tests to be done, 'easiest' part wrt r/o chip)
  few ns collection time achievable with both p and n substrates
- readout chip (challenging)
- cooling (chip power dissipation)
- support & alignment (frequent replacement)

#### Be ready for data taking in 2009