

Multi-Bunch Feedback and High-Current Factories

Operational Experience, Theoretical Limits and Technology Options for future upgrades

J. Fox and D. Teytelman

September 2003

Presented at the Workshop on e^+e^- in the 1-2 GeV range

Alghero

Talk Outline

Requirements for Broadband (multi-bunch) Feedback for High-Current Colliders

History and System design at PEP-II, DAFNE and KEK-B

Operational Issues, theoretical limits, practical limits

Development of beam diagnostics from multi-bunch system data

Technology options in 2003

Implications for high-current machine upgrades

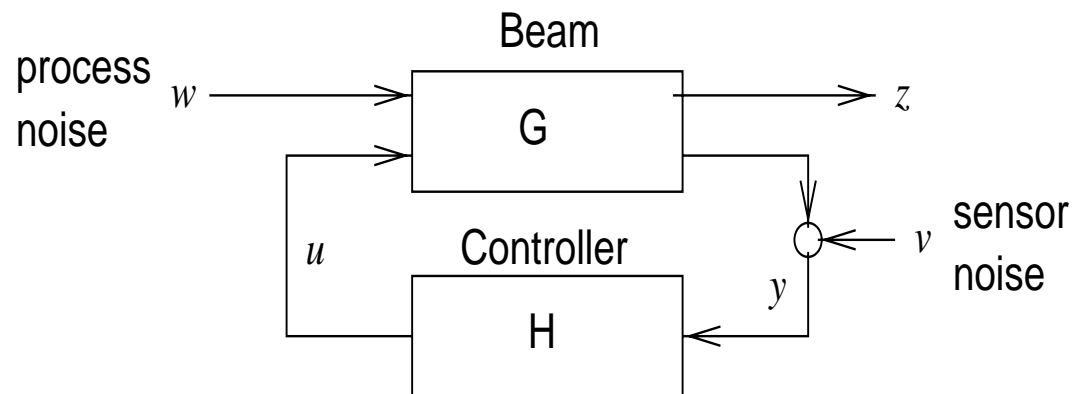
Summary

Feedback Principles - General Overview

Principle of Operation-Feedback can be used to change the dynamics of a system

Longitudinal - measure $\delta\phi$ - correct E

Transverse - measure $(\delta X, \delta Y)$ - kick in X' , Y'



Technical issues

Loop Stability? Bandwidth?

Pickup, Kicker technologies? Required output power?

Processing filter? DC removal? Saturation effects?

Noise? Diagnostics (system and beam)?

Processing Requirements

For instability control, the processing channel must

- extract (filter) information at the appropriate synchrotron or betatron frequency,
- amplify it (a net loop gain must be generated, large enough to cause net damping for a given impedance)
- generate an output signal at an appropriate phase (nominally 90 degrees, but arbitrary if the system and cable delays, pickup and kicker locations are considered)

Some technical issues

- Bandwidth/sampling rate
- DC offset removal from the processing channel (e.g. from DC synchronous phase position, or static orbit offset)
- Saturation on large input errors
- Noise in the input channel (e.g. bandwidth reduction via processing filter)
- Maximum supportable gain - limits from noise as well as loop stability
- Diagnostics (processing system and beam dynamics)

Filter Implementation Options

Terminology

- Time domain - bandpass bunch by bunch filters
- frequency domain - modal selection, notch at Frev

Sampling process suggests discrete time filter (filter generates correct output phase, limits noise, controls saturation)

General form of **IIR filter** (infinite impulse response)

$$y_n = \sum_{k=1}^N a_k y_{n-k} + \sum_{k=0}^M b_k x_{n-k}$$

General form of **FIR filter** (finite impulse response)

$$y_n = \sum_{k=0}^M b_k x_{n-k}$$

wide bandwidth filter - insensitive to variations in machine tune

narrow bandwidth filter - helps reject detector noise

Maximum gain - when noise in front-end saturates DSP processing

History of wideband coupled-bunch feedback, and important technical decisions made by SLAC/LBL/INFN and KEKB

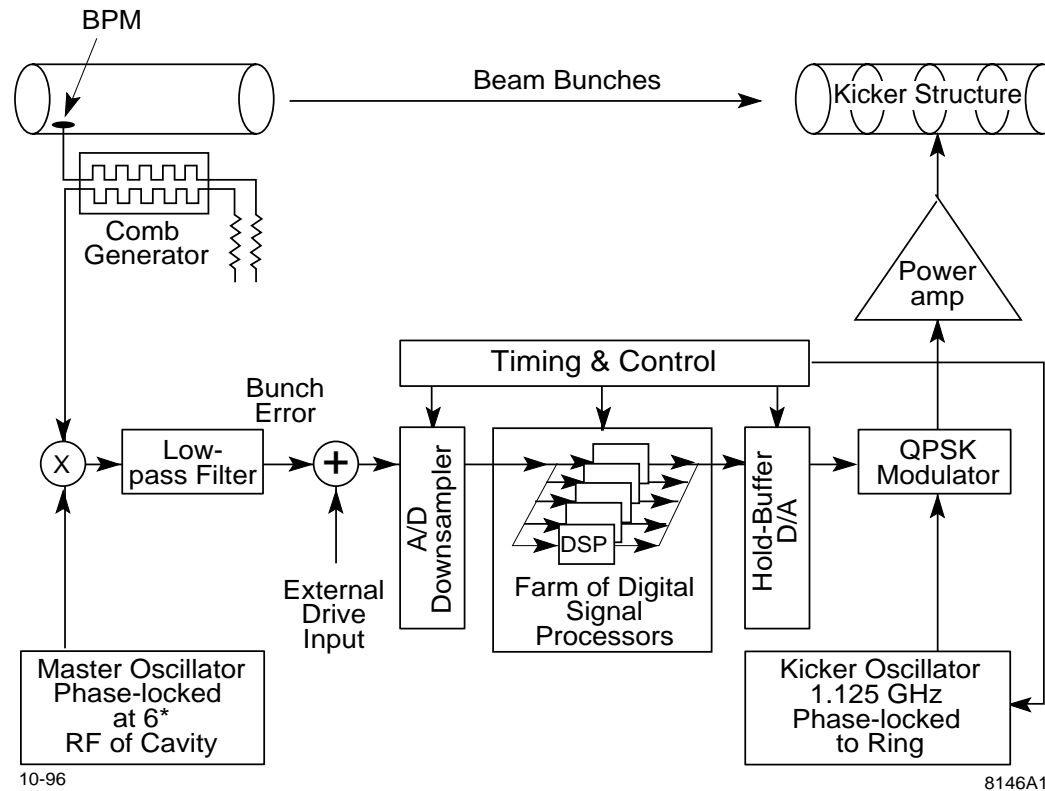
SLAC/LBL/INFN examined a mix of all-analog, hybrid analog/digital, and all digital processing architectures in the original collaboration and study in the early 1990's. At that time, it was decided:

Longitudinal processing was best addressed via a downsampled digital processing channel (where the downsampling better matched the synchrotron frequency to a sampling rate of $1/N$ revolutions). The general-purpose processing channel was implemented in an array of 80 commercial fixed-instruction DSPs (the "farm").

Transverse processing required a full-rate digital processing channel, and we could not see a technical means to implement a fully-programmable filter at the 500 MHz rate. The transverse systems were designed using a two-pickup front end, where the two pickups were separated in betatron phase - the correction signal was computed via a scaled sum of the two pickups, delayed by 1 turn. PEP-II used a digital delay mechanism - the ALS and smaller rings used analog delay cables.

KEKB implemented a non-downsampled full rate digital filter, using a two-tap filter design suggested by Flemming Pedersen. This approach only required addition, not multiplication, though the filter characteristics (limited by DC offset constraints), and control of the output signal phase, are not as general purpose as a true FIR or IIR filter structure. The KEK implementation used full-custom GaAs circuitry to implement an 32 fold demultiplexer/multiplexer channel, with 32 filter channels.

PEP-II/DAFNE/ALS Longitudinal Systems



Front-End Phase Detection at $6 \cdot \text{RF}$ (3 GHz), DAFNE $3 \cdot \text{RF}$

General-Purpose DSP farm (40 - 80 processors)

QPSK-AM output modulator ($9/4$, $11/4$ or $13/4 \cdot \text{RF}$)

High Power Stages 200 - 1500 W (1 - 2 GHz)

Quadrupole instability control

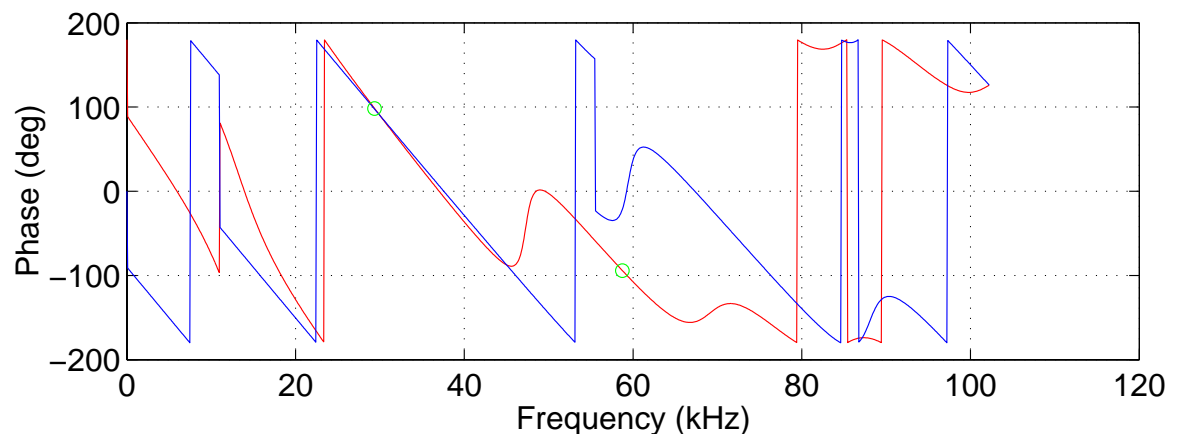
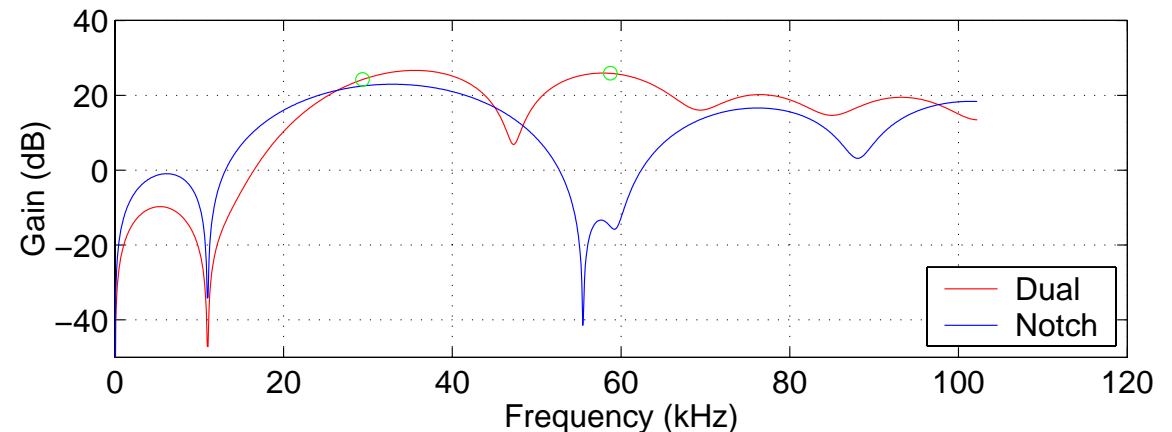
DAFNE e+/e-collider at LNF

- increased operating currents
- quadrupole mode longitudinal instabilities have appeared (the installed system suppresses the dipole modes).

We implemented a novel quadrupole control filter

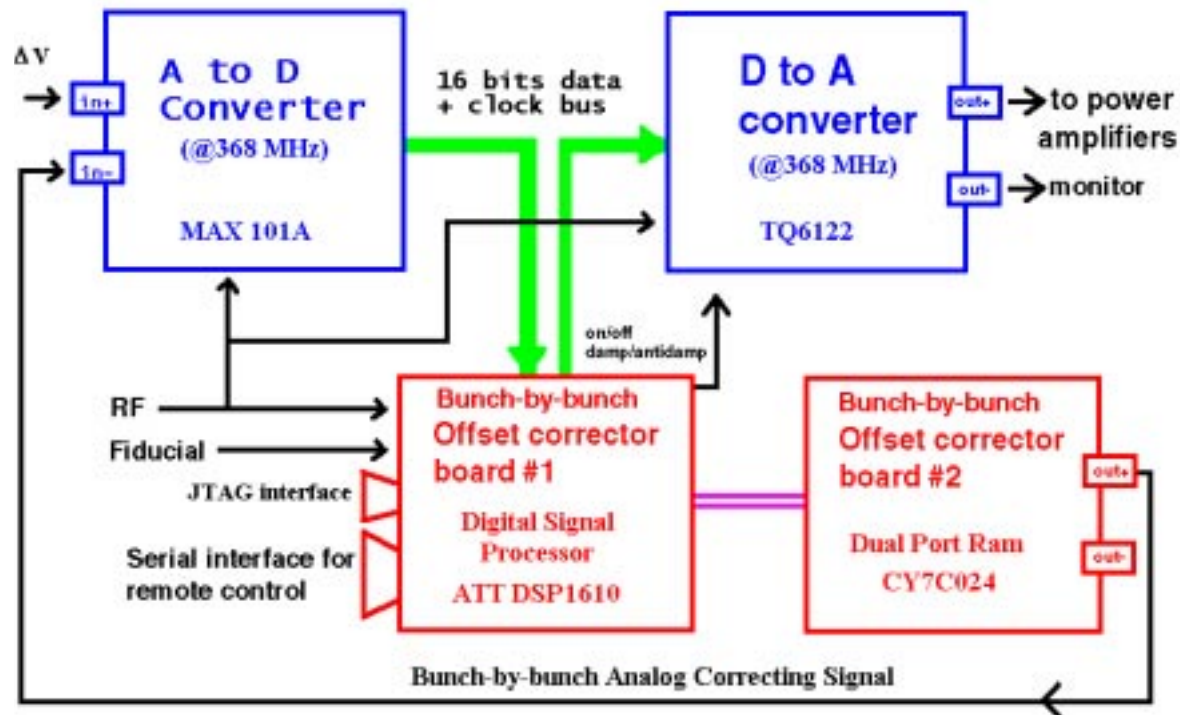
- software programmability of the DSP farm
- two parallel control paths for dipole and quadrupole modes.
- quadrupole control has been successful, allowing a 20% increase in luminosity.

The flexibility of the software-configured control scheme allows this new function without any changes in the installed hardware.



DAFNE Transverse Feedback Processing Channel

A. Drago, et al

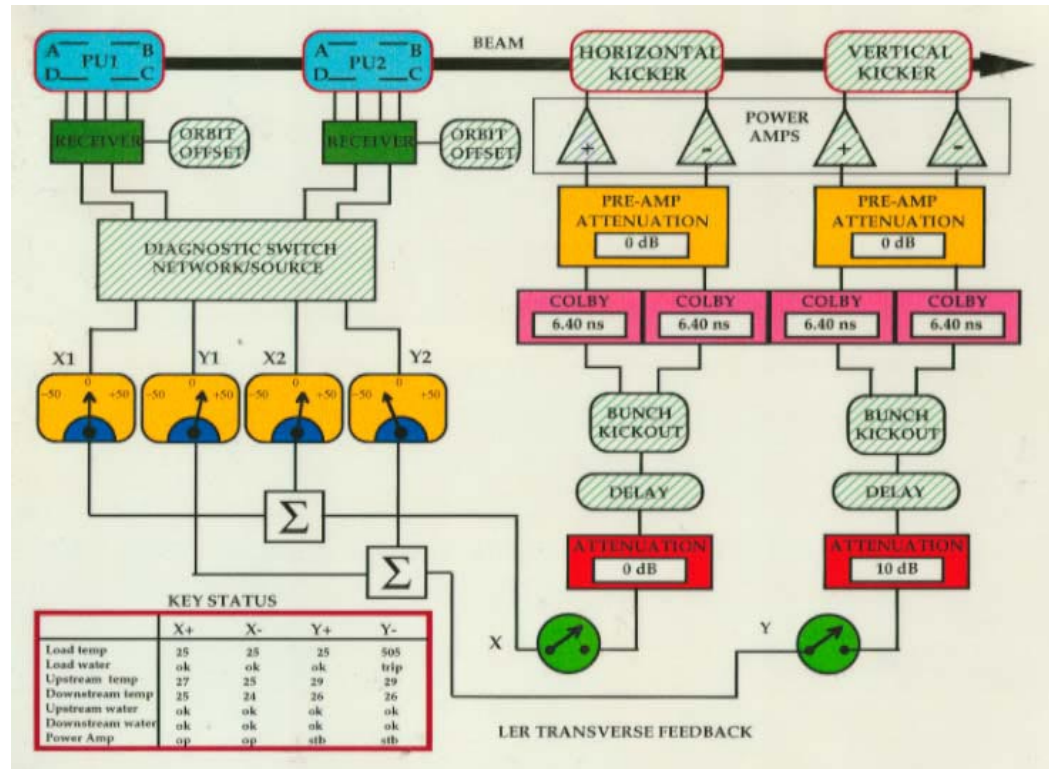


Features - slow DC offset (orbit offset) removal

Digital delay, plus cable delay

BPM pickups selected from set depending on machine tune for proper phase shift and lattice

ALS/PEP-II Transverse Feedback Implementation

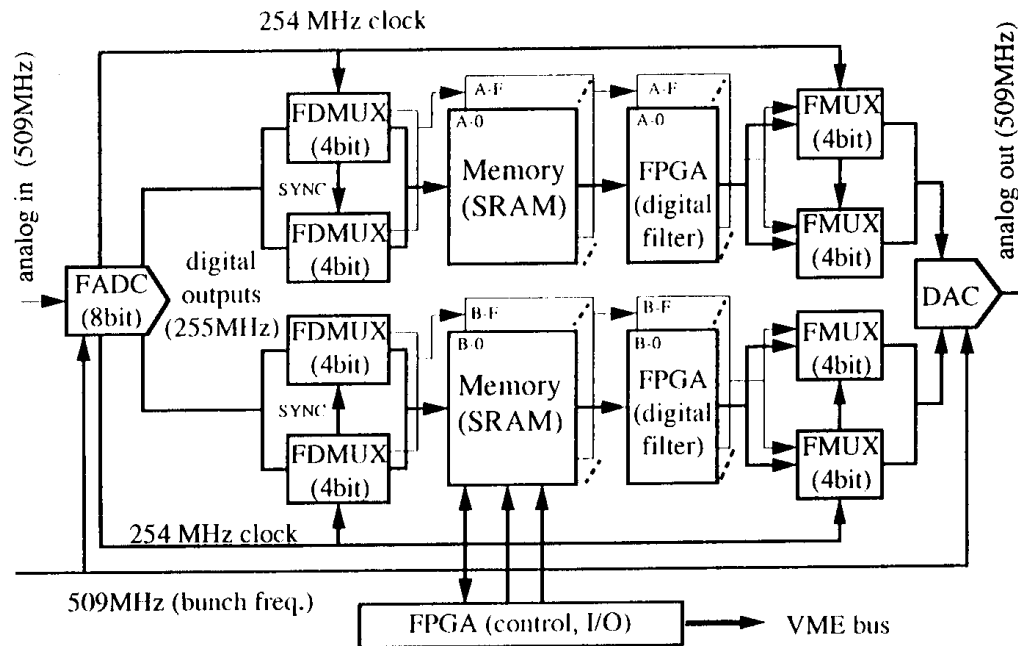


From W. Barry

ALS has Analog 2-tap FIR filter for DC orbit suppression via delay cables and hybrids

Quadrature processing via 2 pick-ups, scaled and summed for gain and phase selection

KEK-B Transverse and Longitudinal signal processing



from M. Tobiyama, et al

2 ns bunch spacing

2-tap FIR structure (fixed 1, -1 coefficients, no multiplier)

32 parallel channels

Kicker Implementations

Transverse -

Essentially all striplines. Length limited by bunch spacing. Operation at baseband (except for KEK-B, using two sets of kickers/amplifiers)

Cornell (CESR) has clever short-circuited design to kick counter-propagating beams. Also a design using a clever duty-cycle modulated kicker driver, as apposed to linear amplifier drive, was explored

Amplifiers - baseband (100kHz - 230 MHz)

Longitudinal - Several designs

Ceramic Gap (UVSOR) - modest shunt impedance

Loaded (damped) Cavity - Designed by LNF-INFN, used by DAFNE, BESSY, PLS, (KEK-B). Easy to cool. Needs circulator. Reasonable shunt impedance. New PEP-II kickers in design/fabrication

Drift-tube structures - designed by LBL Beam Electrodynamics Group, used by ALS, (PLS), PEP-II. Useful in-band directivity. Cooling issues for ampere currents

Operating in 1 - 1.5 GHz band. GaAs power amps (200 - 500 W), also TWT power stages (200 W)

Some installations (e.g. PEP-II) use multiple longitudinal kickers with multiple amplifiers

Stability requirements for the LFB/TFB

LFB/TFB have limitations on the maximum controllable growth rates and maximum synchronous phase transients

Several effects need to be considered to determine LFB/TFB stability

- Growth rates due to the HOM impedances (and resistive wall in transverse case)
 - Proportional to the number of installed RF cavities
 - Proportional to the beam current
- Growth rates due to the fundamental impedance (LFB only, most important for large machines)
 - Proportional to the number of installed RF cavities
 - Depend on the beam current (non-linearly)
 - **Determined by the low-level RF configuration**
- Synchronous phase transient due to the gap (LFB sine detection, TFB cosine detection)
 - Depends on the size of the gap ($\Delta\phi_s \sim L_{gap}$)
 - Depends on the gap voltage per RF cavity ($\Delta\phi_s \sim 1/V_c$)
 - In other words depends on the number of powered cavities and total gap voltage

Ultimate/Practical Limits to Instability Control

What Limits the **Maximum Gain** (e.g. fastest growth rate, or allowed impedance)?

Several Mechanism

I). **Noise** in feedback filter bandwidth, limits on **noise saturation**. Gain is from several stages -

Front End (BPM to baseband signal) gain limited by required oscillation dynamic range, steady-state offsets (synchronous phase transients, orbit offsets)

Processing Block - gain limited by noise in filter bandwidth. Quantizing noise (broadband) is one system limit - noise from RF system or front-end circuitry may also contribute. Narrowband filters help with broadband noise. Broad filter bandwidths help with reduced sensitivity to machine tunes, operating point - or variations of dynamics with current

Power stages - gain scales with kicker impedance, $\sqrt{\text{output power}}$. An expensive way to increase gain (more kickers, more output power).

Output power (actually maximum kicker voltage) determines maximum oscillation amplitude from which linear (non-saturated) control is possible. Saturated behavior is complicated

Ultimate/Practical Limits to Instability Control, part II

II) **Stability of the feedback loop itself**, (e.g. limits on phase shift and gain vs. control frequency)

Ultimate Limits (loop stability) Related to time delay between pickup, processing, and actuator

For circular machines (systems with kick signal applied on later turn than pickup)

limit set by revolution time, fastest growth rates, and filter phase slope over control band

Appropriate for optimal control theory applications

LQR

Robust Control

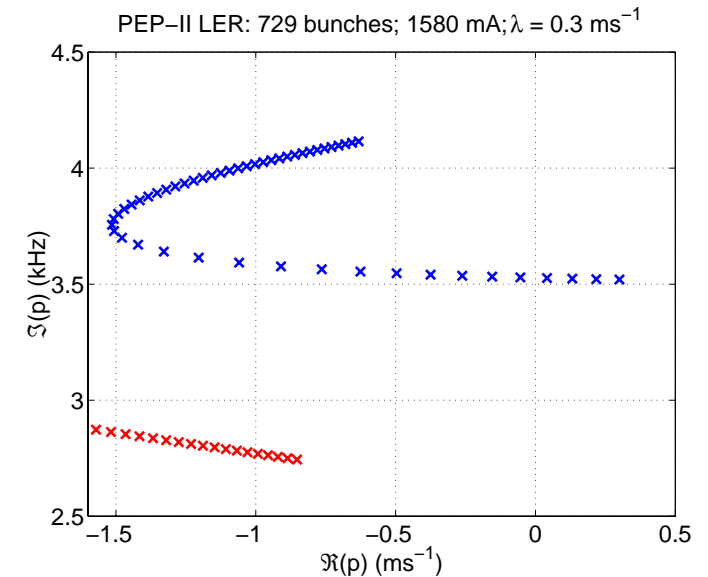
Uncertain Systems

Negative group delay over a portion of the frequency band is possible, but for causal systems you pay the price in increased phase slope away from the negative slope region

Nature of the PEP-II LFB/TFB limitations

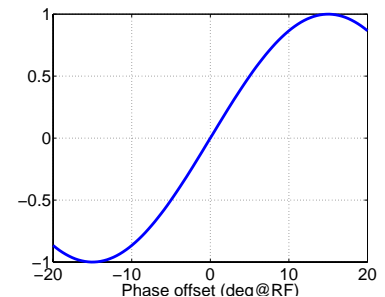
Instability growth rates

- Maximum stable loop gain - depends on controller design, total loop delay. LFB runs FIR/IIR, TFB quad shifter
- Maximum usable loop gain - gain that provides the largest damping. Depends on the same parameters as the maximum stable gain, but is significantly lower
- LFB Feedback systems in PEP-II are currently running near maximum usable gain. TFB? Gain limit from noise or DC?
- Noise floor at the ADC - depends on RF-driven noise level, not a problem for the PEP-II LFB in the current configuration. TFB? DC Offset issues?
- Transient sensitivity - effect of injection and RF feedback transients on control. The sensitivity can be reduced by increasing kicker voltage. Back-end power determines allowed perturbations



Synchronous phase transients (gap transients)

- Front-end of the LFB uses a phase detector at 6th harmonic of the RF. Range of detectable signals is 180 degrees peak-to-peak at $6 \times f_{RF}$ (or 30 degrees peak-to-peak at RF).
- Front-End of the TFB at 3rd harmonic - cosine detection

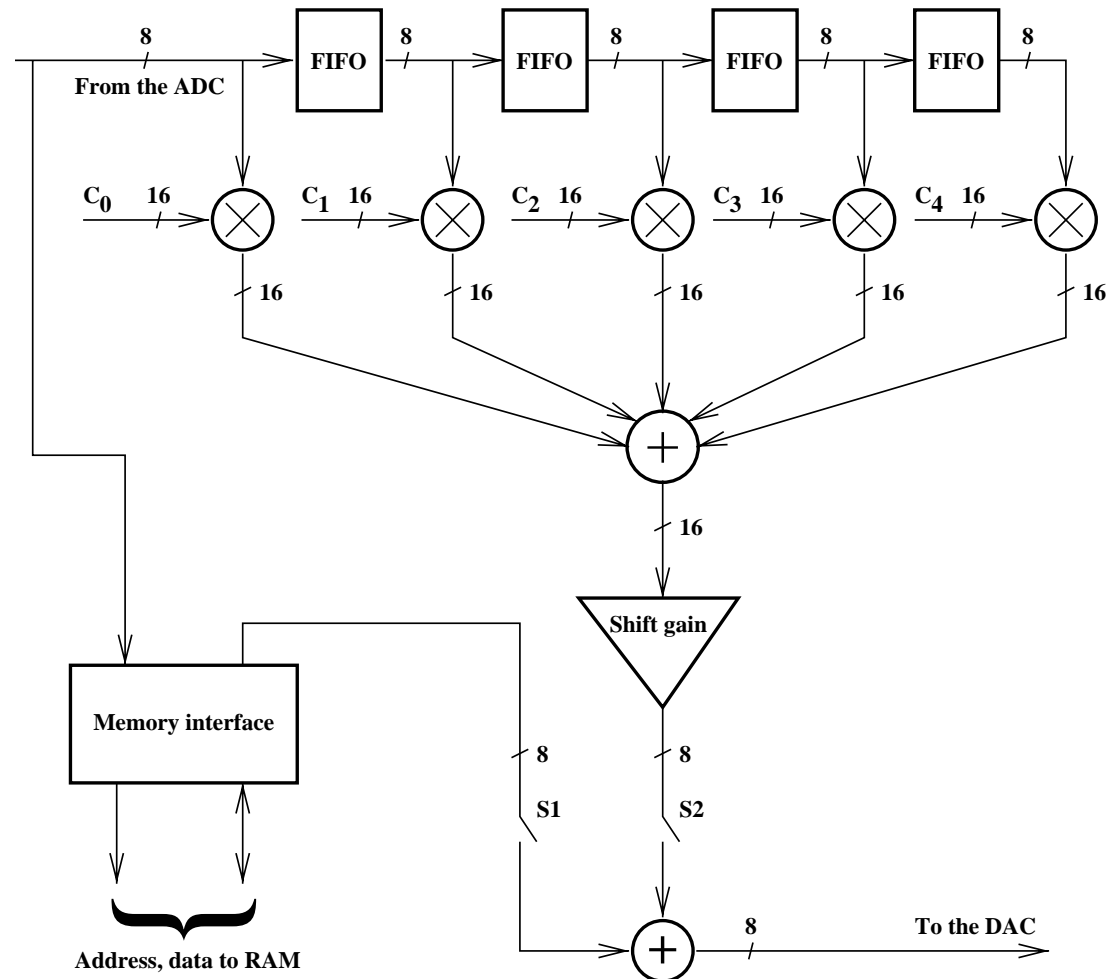


Design of Dedicated Woofer

The existing “woofer” control path is taken after the baseband DSP filter output - it is filtered, re-sampled at a 10 MHz rate, and then transmitted as a digital data stream to selected RF stations. As the signal is derived from the broadband feedback signal, it is not at an optimum phase for best low-mode control after it is delayed an additional turn in the LLRF processing. Additionally, the downsampled processing of the LFB filter adds group delay to the woofer path, that may be a limitation on maximum achievable operating gain.

We are developing a dedicated woofer channel, based on a Xilinx gate array, which samples the baseband phase error signal BEFORE sampling by the broadband processing. This system runs

at a 10 MHz sampling rate, and implements a non-downsampled 12 tap filter. The computed filter outputs are then transmitted to the RF stations via the existing woofer links. Such a lower group delay processing function may be useful in controlling low-modes at higher currents.



Evolution of DSP-based Diagnostics

Original motivation - stabilize coupled-bunch instabilities

- Engineering-level system checks
- Identification of unstable eigenmodes, growth/damping rates at full design currents
- Beam Pseudospectra, Grow/Damp Modal Transients

Second-tier diagnostics

- Predictions of high-current unstable behavior from low-current stable machine measurements (growth/damping rates at design current estimated from low-current commissioning data)
- beam instrumentation - bunch by bunch current monitor, tune monitor, bunch power spectrum (noise) monitor
- Synchrotron tune vs. bunch number - gap transients, tune spread, Landau damping - instability thresholds for various configurations
- Complex Longitudinal impedance vs. frequency from bunch synchronous phases, tune shifts
- Eigenstructures of uneven fills, phase space tracking
- Transverse Motion via DSP Data Recorder/Control

In some ways the development of the beam diagnostics has been the most useful and significant benefit of the use of the programmable technology in the DSP feedback systems.

PEP-II HER Longitudinal instability growth rates at high currents

A parasitic study at 1100 mA

Fastest growing mode is mode -3 driven by the RF cavity fundamental mode.

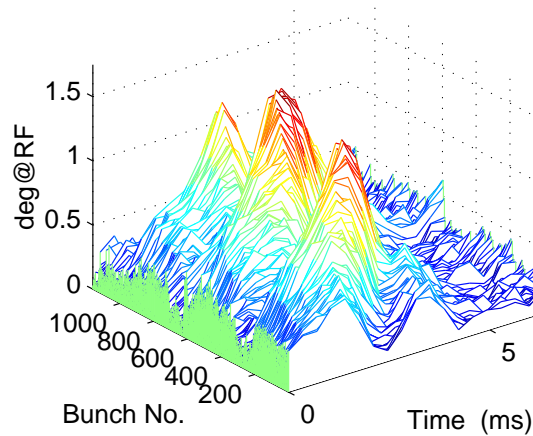
Tune shifts follow the general shape we normally see in simulations

With a 2.5% gap the data is much easier to analyze since there is less mode coupling.

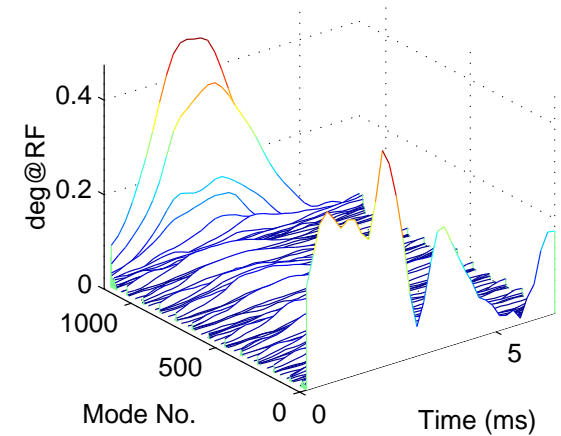
In general, for longitudinal motion, the in-cavity modes (from the fundamental) are roughly 10 times faster than the HOM modes driven by HOM's in the cavities.

The LLRF configurations, and impedance control, are critical in having adequate margin to control these low modes. We use the "woofer" for extra gain.

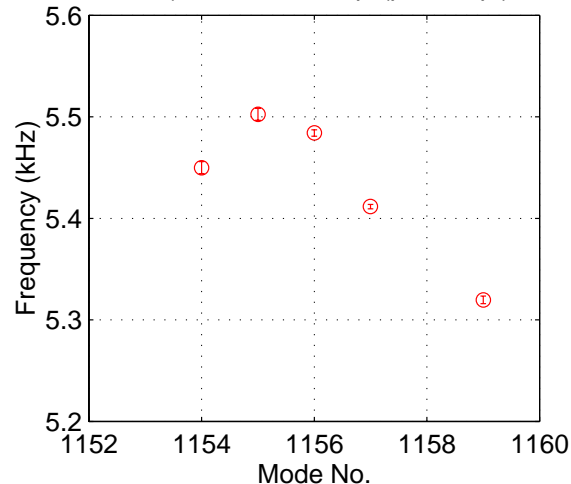
a) Osc. Envelopes in Time Domain



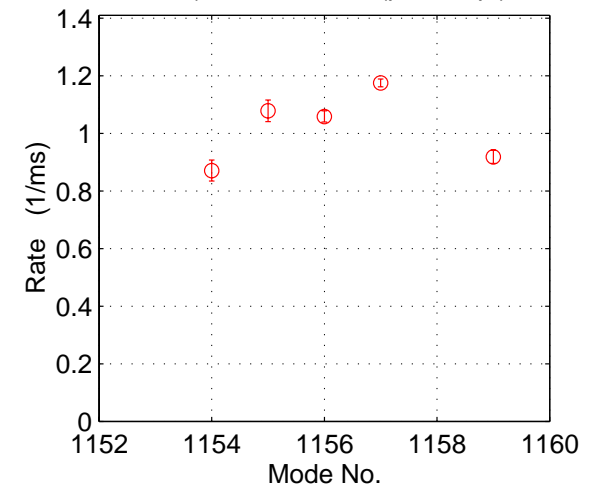
b) Evolution of Modes



c) Oscillation freqs (pre-brkpt)



d) Growth Rates (pre-brkpt)



PEP-II HER:jun1903/021609: Io= 1099.45mA, Dsamp= 6, ShifGain= 3, Nbun= 1160, Gain1= -0.9, Gain2= 0, Phase1= -140, Phase2= -140, Brkpt= 30, Calib= 10.06.

Longitudinal Mode Zero Control

PEP-II is unique, in that the RF system has

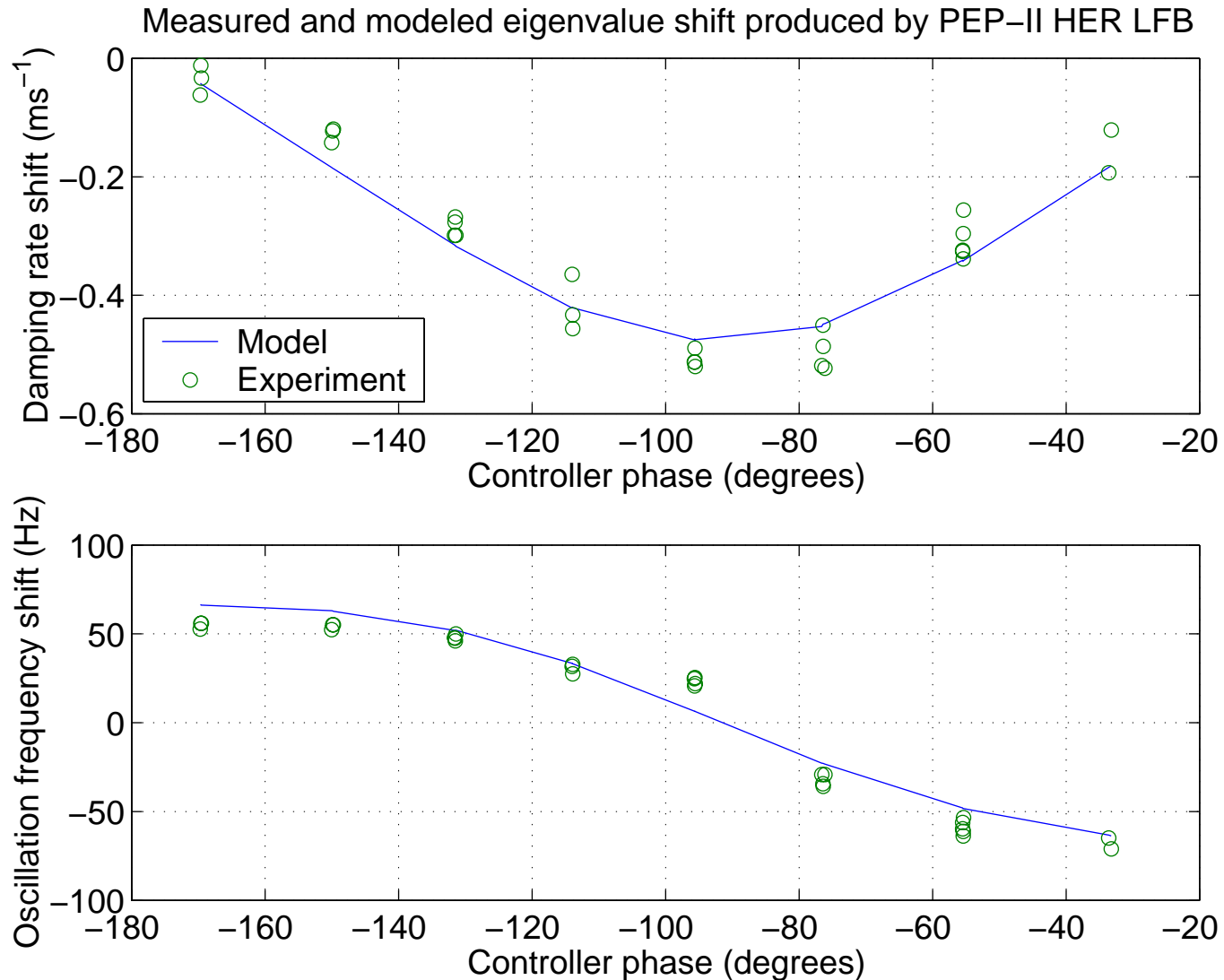
- Broadband RF feedback, which spreads the RF fundamental over 20 revolution harmonics
- Comb-filter RF feedback, to reduce the residual impedance at the synchrotron sidebands around the revolution harmonics within the bandwidth
- A special “Woofers” link with the feedback, in which the lowest frequency feedback signal is equalized and injected back into the RF, increasing the feedback gain for the lowest modes

KEK-B uses both superconducting and room temperature RF cavities, also the ARES energy storage cavity on the room temperature RF cavities. This helps reduce the difficulties with the fundamental detuning driving low negative longitudinal modes - a dedicated mode -1 control loop is used. Future current upgrades will likely also need control of mode -2, etc.

DAFNE has a mode zero RF feedback loop (analog), independent of the broadband feedback to control mode zero at high-currents where the Robinson damping from the cavity detuning is less effective (this was a problem running the FIR filters, as the mode zero frequency was dropping the filter phase began to create positive feedback). Better control with a flatter IIR filter.

PLS, BESSY - mode zero controlled through broadband feedback - sets a tight tolerance on master oscillator phase noise. Shift in mode zero oscillation frequency vs. current requires a very careful specification of the control filter (special IIR designs in use at ALS/BESSY/DAFNE)

Longitudinal Model and Experimental Verification



Upgrades and High-Current Heating issues, monitoring

Both the PEP-II TFB and LFB have numerous thermocouples on the vacuum components and cables, feedthroughs and some high-power loads. The water-cooled components additionally have flowswitches to monitor water flow.

PEP-II has had cable fires, arcing and destruction of high-power kicker feedthroughs.

The LFB also has high-power monitoring in:

Amplifier reverse power meters and protection trip circuits (causes beam abort)

Load power monitoring via directional couplers and diode power detectors which are logged by the operations group.

A special load power derivative trip circuit was designed and fabricated as a graduate student project, but never commissioned. Idea was to have fast (sub millisecond) trip if the load power level went up or down rapidly. Had to gate the trips with current to not trigger on beam aborts or other fast beam loss. Might be worth commissioning this.

Both LFB and TFB have filters between the beam-line components and the power amplifiers to reduce out-of-band power going backwards into the amplifier outputs. New Cavity-style longitudinal kickers will require circulators, likely in addition to the existing absorptive filters.

Technologies and Options

The last decade has seen explosive development of general purpose DSP chipsets, special DSP EPLD devices, and extensive commercial development of DSP software and design tools.

The RF and microwave circuit technology developed for wireless telecommunications markets has offered an unprecedented array of monolithic and highly integrated RF functions (amplifiers, modulators, mixers, etc.)

Tremendous opportunities, and some pitfalls

#1) Commercial pressures have produced some very integrated functions in the most popular communications bands- but only in specific frequency bands

#2) Commercial pressures have forced some manufacturers to abandon mature product lines, leaving some traditional frequency bands and functions with limited choices

#3) Commercial pressures have brought on rapid product obsolescence, availability concerns for designed-in functions. A very poor match of commercial product life cycles to accelerator design-commissioning- operation cycles

Promising Areas for Research

500 Ms/sec. to 1.5 Gs/sec. Digital Signal Processing

Reconfigurable EPLD functions with DSP cores, built-in RAM functions (Xilinx Virtex-II series)

These developments suggest that a general-purpose, software configured processing architecture could be developed, with applications to many feedback and instability control problems at a range of circular machines. Applicability to many dynamics diagnostics (tune measurement, impedance measurements, tune vs. bunch number, trajectory measurements, transverse HOM impedance characterization, bunch by bunch current measurements, etc.)

Function	Performance (from Xilinx)
MACs per second	600 Billion
FIR Filter - 256-tap, linear phase, 16-bit data/coefficients	180 MSPS @ 180 MHz
FFT - 1024 point, complex data, 16-bit real & imag. output	<1 μ s @ 140 MHz

Throughput of 1 Gs/sec. does not mean 1 ns of group delay - such processing blocks would be pipelined, with significant time delay from input to output.

Promising areas for research, II

Very low group delay processing blocks

Such functions would still use a basic FIR/IIR topology, but have the lowest possible group delay (throughput delay).

Applications to feedback, feed-forward systems

One future application - stabilization of transverse offsets or transverse position vs. bunch number in single-pass colliders with trains of bunches. Basic idea - use error signal derived from initial beam-beam deflections to rapidly compute a feed-forward correction used to steer the rest of the trains into collision.

Speculative application - instability control systems for circular machines which correct within a turn, using error information from bunch N to correct on bunch $N+M$, where M is less than the harmonic number. The error filter would be essentially estimating motion of the bunches based on modal information and motion detected from the bunches. Also it is possible to use a fast channel, combined with a fast cable plant that cuts across the ring for low group delay feedback.

Likely implementations are electro-optic. Such systems should also be programmable, in that an adaptive controller might adjust the feedback filter(s) or tap weightings slowly to converge on an optimum correction filter.

Promising areas for research, III

Development of wideband Actuator (kicker) structures

Any feedback scheme requires actuators - existing kickers have bandwidth limitations restricting use to dipole modes, finite gains and all have power level restrictions.

Higher bandwidth devices could control quadrupole, higher modes of oscillations

(interesting use of finite bandwidth kicker to control both dipole and quadrupole longitudinal modes independently demonstrated at DAFNE)

Development of high power RF amplifiers for actuators, development of high-power RF and kicker signal delivery components

Existing approaches use costly power amplifiers based on parallel medium power GaAs FET technology

Existing vacuum kicker components, feedthrough and power cabling components might not be up to higher-current upgrades in terms of beam induced heating

Technology options in 2003

Do we really need 1 GSPS?

We think we really need **1.5 GSPS!**

Several machines in design right now are considering bunch repetition rates above 1 GHz.

- Photoinjected Energy Recovery Linac design at BNL is using TESLA superconducting 1.3 GHz RF cavities.
- IR ring at LBNL is considering 1-1.5 GHz RF.
- PEP-II is considering upgrade to 952 MHz RF

Even for the 500 MHz and lower RF frequencies it is useful to be able to get two samples per bunch.

- I&Q detection using a single ADC
- Supporting a dual pickup transverse front-end

2003 technology supports very high-speed FPGA architectures, with special dedicated DSP functions

- High speed logic
- high speed multipliers as function block
- design tools for DSP functions

Gboard Processing Channel Specifications

We (SLAC/KEK/LNF) are designing a general-purpose feedback signal processor as a single VME64X module:

- Transverse bunch-by-bunch control at KEKB, PEP-II, DAFNE and others
- Longitudinal bunch-by-bunch control at KEKB, PEP-II, DAFNE, et al
- Transient-domain diagnostics features (e.g. instability growth/damping rate measurements)
- Fast bunch and beam instrumentation (e.g. bunch by bunch current monitor, tune monitor, gap transient/synchronous phase measurement)
- Support bunch spacings down to 0.66 ns - sampling at 1.5 GHz.

The baseband processing channel is useful for transverse processing using two pickups (e.g. quadrature pickups) or single pickup approaches (filter adjusts phase shift of kick)

The fast sampling rate can implement two sample/bunch processing for true I&Q front end processing (research follow-on efforts)

This core function is general purpose, and re-configurable into a variety of signal processing and instrument functions - the reconfigurable Xilinx FPGAs define the exact algorithm. With the 1.5 GHz sampling rate this core function would be applicable to several other accelerator processing needs, including NLC damping rings, numerous existing and proposed light sources, and several recirculating linac proposals.

Gboard Processing Channel Specifications, Cont.

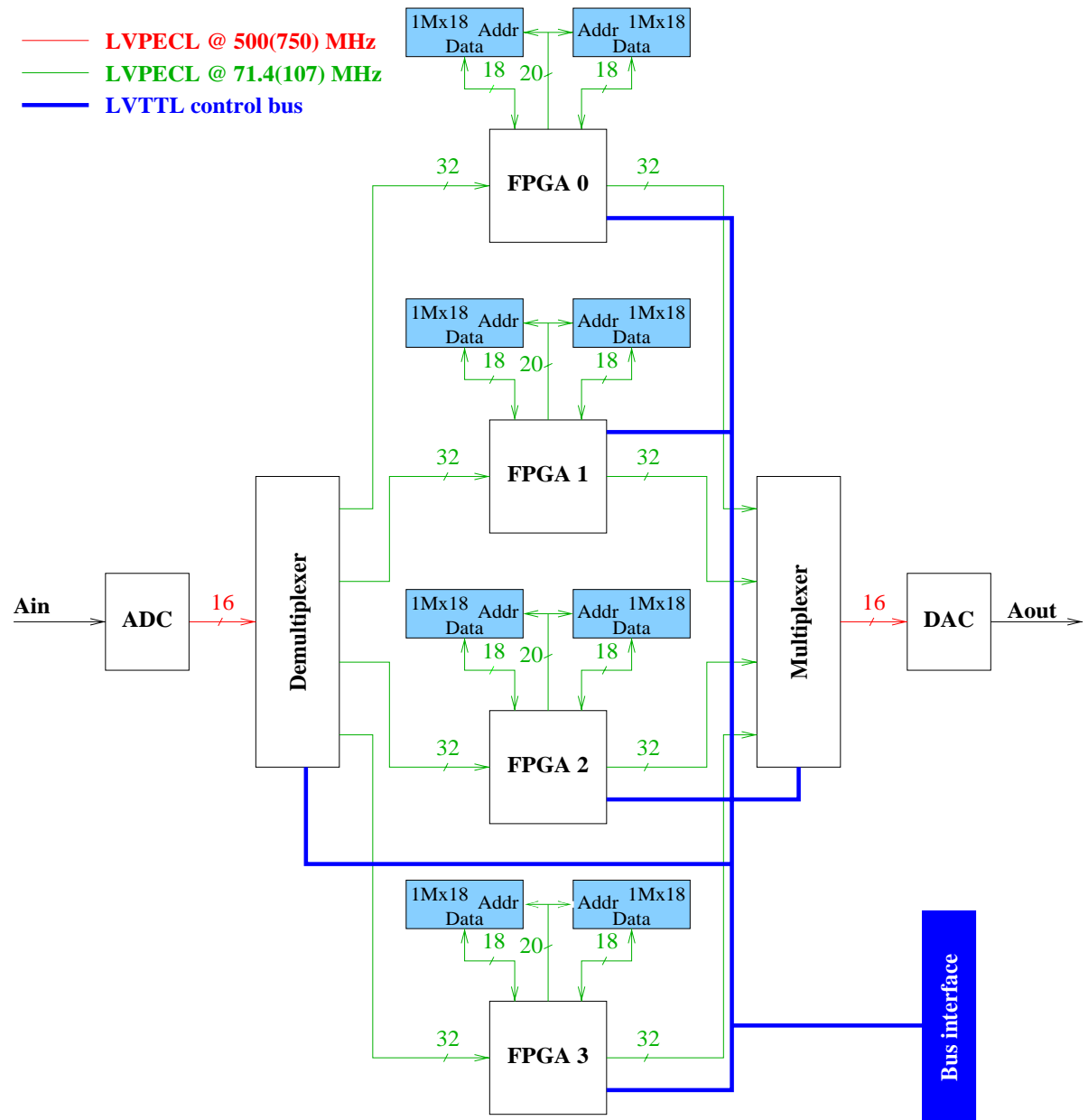
The basic structure of the processing channel is a high speed multiplexed parallel processor, with single input and output channels. The architecture is optimized to do cyclic processing, as in a storage ring, where the computation of the output for channel N depends on the past history of channel N. However, the re-configurable Xilinx gate arrays could support a variety of functions, including a prompt high-speed feedback/feedforward channel, consistent with the pipeline delay in the A/D and processing stages.

- Support arbitrary harmonic numbers (may be OK to support only even numbers?).
- Independent processing for all bunches on all turns - required for transverse feedback.
- Diagnostic memory capable of holding 20 ms of data at the full rate
- Support downsampled processing - reuse the hardware to get longer filters
- Support downsampling for diagnostics for studying slow events
- Support long FIR or IIR filters

In longitudinal feedback non-downsampled processing allows one to better filter out the broadband noise, reduces loop delay somewhat. For example, the processing downsampling by 30 has 15 turn (0.5 sample) delay added to the filter group delay (90 turns for 6 tap filter) - a total of 105 turns. Running the same filter at full rate (180 taps!) the delay is only 90 turns. Of course, this extra complexity requires more computational resources.

GBoard 1.5 GS/sec. processing channel

- Next-generation instability control technology
- SLAC, KEK, LNF-INFN collaboration - useful at PEP-II, KEKB, DAFNE and several light sources.
- Transverse instability control
- Longitudinal instability control
- High-speed beam diagnostics (1.5 GS/sec. sampling/throughput rate)
- Builds on existing program in instability control and beam diagnostics.
- Significant advance in the processing speed and density previously achieved.



Hardware description

Baseband architecture with 1.5 GHz maximum processing rate implemented as a single VME64X module.

Data Flow Processing is implemented in 4 Xilinx Virtex-II FPGA devices.

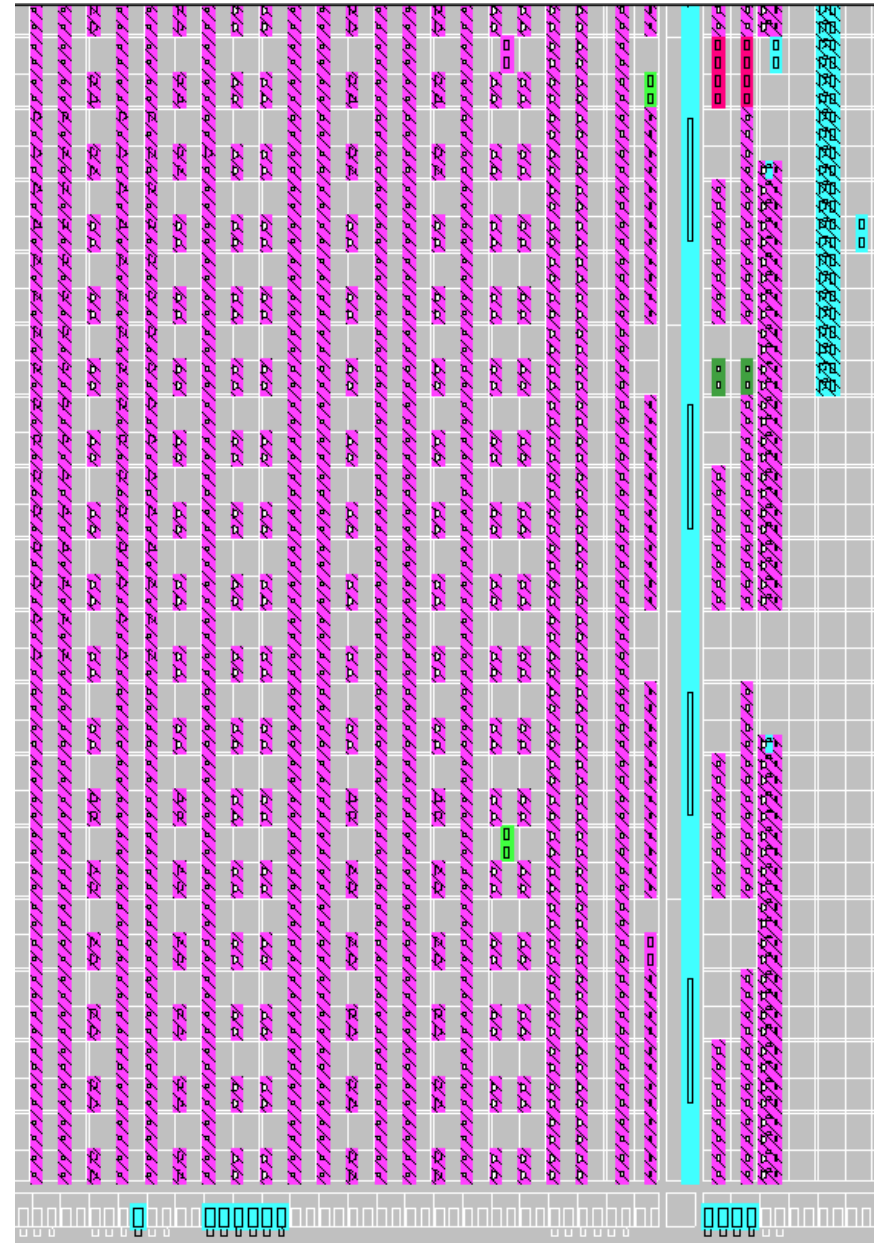
Each chip handles 4 data samples in parallel. With uneven stepping parallel stream alternates between 16 and 14 samples (94-107 MHz clock rates at 1.5 GSPS).

Use Xilinx Virtex-II FPGA XC2V8000

- 112 × 104 CLB array
- 3024 Kbits of RAM
- 168 18 × 18 multipliers - up to 210 MHz clock

Each FPGA controls two synchronous SRAMS of 512K x 36

System can acquire 7 x 2 x 1M=14M samples of transient data (worst case) - this corresponds to 14 ms data record at 1 GHz.



Example of PEP-II/KEKB- B /DAΦNE processing

KEKB and PEP-II are the most processing intensive machines.

Table illustrates processing loads and limitations of the FIR algorithm.

Table 1: PEP-II, KEBB, and DAΦNE processing

Parameter	PEP-II	KEKB	DAΦNE
RF frequency, MHz	476	508.9	368
Harmonic number	3492	5120	120
Stepping selection	213@16, 6@14	320@16, 0@14	4@16, 4@14
Groups per turn	219	320	8
Multiplier limit on FIR filter taps	42	42	42
FIR processing rate for I&Q sampling, MHz	34	36.35	26.3
Full I&Q channel rate	68	72.7	52.6

In case of DAΦNE multipliers can be used several times per sample to make longer FIR filters

Detailed Design and Development Issues

Our initial KEK-SLAC design collaboration has shown the feasibility, and the critical high-speed signal processing channel is verified via functional and timing verification - what's left to do?

Signal processing - verify functioning of downsampling features (that allow best use of the processing capability for longitudinal processing in some situations)

Remaining tasks - the real detailed engineering

Control interface, user interface

High-speed timing and clock distribution design

physical layout, circuit PC board design, controlled impedance design

(the physical layout, delays, skews, etc. are NOT simulated in the board-level simulation)

Packaging format - VME64X? 400 mm depth? What supplies to use?

Component choices - largely made. Issue of use of Triquint D/A?

Board size issues - density, thermal management, use of BGA technology (limits useful board size)

Front panel - connectors? Monitor points or functions? Temperature monitoring? Shutdown?

Initial module prototype with baseband processing - use existing detection, front end and back-end functions as they are implemented. Later implement new VME64X functions?

Summary

The three factories (DAFNE, KEK-B and PEP-II) all have significant experience running these multi-bunch instability control systems. Each set of system designers has achieved success for the existing operating currents

The **instabilities** themselves are proportional to current, and proportional to the driving impedances. Running these facilities at higher currents requires some analysis to understand the practical limits of these instability control systems.

The technology of these systems may evolve, but the **fundamental limits** to the performance of these systems, e.g. the **saturation effects from noise** limiting the gain, and the limits on gain and phase from **loop stability** of the feedback loop, are the central limits we must never ignore.

PEP-II is pushing the group delay limits in the control of the low in-cavity longitudinal modes, and has some operational history with power dissipation and thermal management of the kicker structures.

The diagnostics possible with the programmable DSP based systems are very useful in validating dynamics and understanding the performance of the instability control. They also provide many very **unique accelerator diagnostics** (such as measurement of complex HOM impedances). The **flexibility** of these systems has been an opportunity to address several control needs as the accelerators were modified (such as the addition of harmonic cavities to the ALS, requiring novel IIR control filters, or the quadrupole mode control at DAFNE)

The new technology in development (e.g. the Gboard effort) offers faster, more complex options.

Acknowledgments

Thanks to D. Andersen, L. Beckman, P. Corredoura, N. Hassenpour, M. Minty, C. Limborg, S. Prabhakar, W. Ross, J. Sebek, D. Teytelman, R. Tighe, U. Wienands, A. Young (SLAC), H. Hindi, I. Linscott (Stanford), M. Tobiyama, E. Kikutani (KEK), A. Drago, F. Marcellini, M. Serio (LNF-INFN) and W. Barry, J. Byrd, J. Corlett, G. Lambertson and M. Zisman (LBL) for numerous discussions, advice and contributions.

The PEP-II digital processing architecture and modules were skillfully designed and developed by G. Oxoby, J. Olsen, J. Hoeflich and B. Ross (SLAC) - System software was designed and coded by R. Claus (SLAC), I. Linscott (Stanford), K. Krauter, S. Prabhakar and D. Teytelman (SLAC)

The wideband longitudinal kicker for ALS and PEP-II was designed and developed by F. Voelker and J. Corlett (LBL). The kicker for DAFNE was designed by R. Boni, A. Gallo, F. Marcellini, et.al.

Special thanks to Boni Cordova-Grimaldi (SLAC) for fabrication expertise and to the ALS, SPEAR, PEP-II, and DAFNE operations groups for their consistent good humor and help.

Work supported by U.S. Department of Energy contract DE-AC03-76SF0051