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THE SPARC_LAB SYNCHRONIZATION SYSTEM UPGRADE

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Abstract

This paper report the recent results obtained in the SPARC LAB synchronization system after a global upgrade. We have achieved two main results: (i) the replacement of the electronics for the stabilization of the photocathode laser oscillator repetition rate, (ii) the integration of the FLAME interaction laser repetition rate stabilization unit in the SPARC LAB synchronization system and (iii) the integration of the photocathode laser PLL in the control system included a control room GUI. The design, test and commissioning these new HW and software solutions are extensively treated in this document. The final result was very significant in the machine operation since we pushed the system to work at its best. We report about the time jitter measurement of the single sub-systems respect to the main reference RF oscillator and also jitter measurement of the electron bunch arrival time at different locations along the machine. Values well below $100 f_{s_{RMS}}$ has been observed. We met the stringent specifications required to realize some advanced experiments involving RF rectilinear compression, interaction of short power lasers pulses with electron bunches, advanced FEL experiments and particle driven plasma wave acceleration [1]. The last chapter describes the new features of the control system software.

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1 The present SPARC LAB synchronization system layout

The synchronization is presently provided by an analog RF reference signal distributed through a coaxial cable network, and client lock-in is based on electronic PLL implementing μ -wave techniques. In the near future we plan to perform much more demanding experiments, such as external injection of very short electron bunches in a laser-driven plasma wave for post acceleration. The synchronization request is dramatically more stringent in this case, at level of $\approx 10 fs$, which requires a technological jump to optical techniques. To reach this new frontier we are preparing the migration of the SPARC_Lab synchronization system from electrical, cable based distribution and lock-in, to full optical, fiber based, architecture.



Figure 1: SPARC_Lab electrical synchronization system schematics

1.1 Reference generation and distribution

The present SPARC_Lab synchronization system schematics is shown in figure 1. The Reference Master Oscillator (RMO) is a custom low-noise RF source providing the main RF frequency 2856MHz, together with the $2 \times RF$ reference 5712MHz to drive in

the next future a pair of C-band accelerating sections under installation along the linac, and the $3/4 \times RF$ reference 2142MHz which is used to downconvert to baseband the output signals of BAM (Bunch Arrival Monitor) and LAM (Laser Arrival Monitor) resonant cavities [4]. The RF reference source, using an high performance OXCO oscillator, shows itself an integrated phase noise of $\approx 60 fs$ in the $10Hz \div 10MHz$ range around the 2856MHz carrier, as shown in figure 2. This means that the clients locked to this reference will likely exhibit an integrated phase jitter of the same order or greater. However, what finally counts for the facility performances is the relative phase jitter among the various lasers and RF clients, and we consider the spectral purity of our RF source adequate for our present experimental program.



Figure 2: SSB phase noise spectrum of the SPARC_LAB RMO

The RF source 2856MHz frequency is distributed to the SPARC S-band RF power plants, to the RF receiver board which demodulates to baseband the linac RF signals sampled along the power distribution waveguide network around the accelerating structures, and to the optical oscillator cavities of both the photocathode and interaction lasers to precisely lock their pulse repetition rates to a common reference.

1.2 Lock of the RF accelerating fields

The reference signal feeds the 2 S-band klystrons power plants, the first one driving the SPARC RF gun and the TW (Traveling Wave) accelerating section #3, the second one driving the TW accelerating sections #1 and #2 through a pulse compressor system. Also a new C-band (5712MHz) klystron has been integrated in the LLRF system to drive the new C-band accelerating structures that will substitute the S-band accelerating section #3

[2]. The output of both S-band klystrons are phase locked to the reference by a fast, intrapulse feedback system [3] capable to reach its steady state within the RF pulse duration of $\approx 4\mu s$. The RF phase jitter at the klystron output is reduced to $\approx 50 f s$, a level comparable with the resolution of our RF measurement hardware. Slow pulse-to-pulse feedback systems are also in operation to compensate long term drifts of RF phase related to thermal variations in the Linac hall and klystron gallery.



1.3 Lock of the FLAME interaction laser

Figure 3: Schematics of a standard laser client synchronization technique

The SPARC_Lab facility integrates the SPARC linac and the FLAME interaction laser capable to deliver 10Hz infra-red (TiSa, 800nm) pulses with energies > 1J and durations < 30fs, i.e. in the 100TW peak power regime. Such a laser is also a scientific instrument for standalone experiments, and it is used in combination with the linac for experiments of electron-photon interaction. Recently, the first experiment of this category has been performed, which has shown the evidence of production of X-rays by electronphoton Thomson backscattering. The laser is synchronized at the optical oscillator level by mean of a standard locking technique. The oscillator frequency is RF/36 = 79 +1/3MHz and it is locked to the RF reference by means of an electro-mechanical PLL shown in figure 3. The length of the optical cavity of the laser oscillator is adjusted by a piezo-controller moving a mirror, so that the laser oscillator behaves like a VCO (Voltage Controlled Oscillator). A sample of the oscillator pulse train illuminates a photodetector with adequate bandwidth, and the required harmonics (n = 36, f = 2856MHz) of the signal is extracted with a bandpass filter. The signal is then phase compared to the reference, and the error signal is treated with a low frequency amplifier to shape the loop transfer function and finally connected to the piezo-motor driver to lock the phase and the frequency of the optical cavity. A stepper motor provides a coarse mirror positioning in order to operate the piezo-motor at the center of its dynamic range. In the FLAME case all this hardware is embedded in the control electronics provided by the manufacturer (Amplitude Systmes). The measured residual SSB phase noise of the FLAME oscillator is shown in figure 4, corresponding to an integrated absolute jitter of $87f_{s_{RMS}}$ in the $10Hz \div 10MHz$ band. The repetition rate of the high energy laser pulses is 10Hz, which means that one oscillator pulse every 100ms is selected and amplified. All the oscillator pulses, including the selected and amplified ones, are synchronized to the reference.



Figure 4: SSB phase noise spectrum of the FLAME oscillator locked to the RMO signal

The loop phase detector works at the 2856MHz, the 36th harmonics of the laser repetition rate. In general high frequency phase detection is more accurate and leads to better PLL performances. However, when locking a low-frequency oscillator with a PLL working on its Nth harmonics, there are N possible final phase states of the oscillator. This uncertainty may affect the facility synchronization whenever more lasers are locked to a common harmonic reference. We chose to prevent such a problem upgrading the system and putting extra conditions to the lock of the SPARC photocathode laser (see paragraph 2.2).



Figure 5: SSB phase noise spectrum and integrated jitter of the MIRA laser oscillator with different PLLs

2 System upgrade

2.1 Lock of the photocathode laser

The SPARC linac beam originates in an RF gun cavity, where the electrons are extracted from a metallic photocathode by an UV energetic laser pulse at repletion rate of 10Hz. The PC (Photo Cathode) laser define the launching time of the beam, and together with the RF fields which control the capture processes, define the time of arrival of the bunch at the end of the linac. The PC laser synchronization to the reference is made exactly in same way already described for the FLAME laser. The PC laser oscillator (MIRA model produced by Coherent Inc.) has the same repetition rate as the FLAME one (79 + 1/3MHz)and was originally equipped with its own synchronization hardware and software. The laser has been operated with its original control electronics for few years, with a measured jitter in the $200 \div 300 \, fs$ range. Recently we replaced the phase detection electronics and the error signal amplifier of the PC laser PLL to improve its performance. The PLL front end has been redesigned to operate at the main SPARC RF frequency (2856MHz). A new photodiode with > 3GHz bandwidth has been installed to monitor the phase of the MIRA pulse train. A new and dedicated error amplifier based on OP AMP has been designed, built and tested. In particular, we found very effective to increase the multiplicity of the PLL integrator. With a proportional error amplifier the PLL shows a transfer function with a single pole in the origin (f = 0), i.e. a simple integrator frequency response. The MIRA measured SSB phase noise spectrum for this configuration (PLL1) is reported in figure 5. The spectrum shows a bump in the 15kHz region, and the jitter integral value is $\approx 230 fs$. By adding one (PLL2) or two (PLL3) more poles in the origin (with corresponding zeroes near the loop cutoff frequency to preserve the loop stability) the MIRA noise spectrum is reduced and the integrated jitter is lowered to $\approx 70 fs$, dominated by the intrinsic noise of the reference. The error amplifier circuit corresponding to PLL3, which gives the best performances in terms of MIRA jitter, is shown in figure 6.



Figure 6: Error amplifier providing a triple integrator frequency response (PLL3)

2.2 FLAME and PC laser low frequency lock

To achieve a good sensitivity in the phase comparison, both the laser PLLs work at the main linac frequency 2856MHZ. Then, every 100ms, only a pulse of the 79 + 1/3MHz(RF/36) train is amplified. The selection of the pulse is made by using an HV electrooptical modulator (typically a Pockel's cell) driven by the 10Hz machine trigger, conveniently delayed. If the two lasers locking system are left independent, the relative delay can change every time they are locked, since the synchronization is made at the 36th harmonic of the repetition rate and each laser can lock at 36 positions between two consecutive pulses, where the error signal is zeroed. To avoid this, the error amplifier OP AMPs are also used to gate the MIRA PLL, i.e. to condition the MIRA lock to the actual FLAME pulse temporal position to avoid the uncertainty arising from the harmonic PLL. In practice, the relative phase between MIRA and FLAME is measured at the laser oscillators fundamental frequency 79 + 1/3MHz, and the OP AMPs of the MIRA PLL are enabled only if the measured phase is within the $\pm 5^{\circ}$ range (i.e. 1/36 of the entire 360° range). By doing this the MIRA lock is aligned with FLAME and the uncertainty is removed. The coarse relative shift between the 2 lasers is controlled by a phase shifter inserted in the FLAME channel upstream the 79+1/3MHz phase detector. The fine temporal shift between the 2 lasers is controlled by two motorized delay lines (trombones) moving the phase of the 2856MHz PLL reference. The schematics of the MIRA-FLAME synchronization system is shown in figure 7.



Figure 7: Block diagram of the MIRA-FLAME synchronization system

3 System performances

The system upgrade has been very effective in the stability of the accelerator operation. In particular, using a RF compressed beam, we are sensitive to the accelerating field phase inside the accelerating section #1, that affect the characteristics of the beam (in terms of longitudinal phase space) at the linac end. The jitter of the beam respect to the RF phase is in fact a combination of the RF phase noise inside the accelerating structure and the PC laser time of arrival on the cathode. To characterize the longitudinal stability of the electron beam we used two independent measurement setups by means of a RF deflector [4] and an EOS system [5]. We report about the measurements done on a RF compressed beam, since the EOS setup needs high peak current beams to have a good resolution. In this special acceleration regime, the particle are longitudinally pushed to follow a certain phase of the RF field, reducing the contribution of the PC laser arrival time on the cathode



Figure 8: Diagnostics on the electron beam time jitter

to the total e-bunch time jitter. The RF deflector measurement is performed by observing the vertical jitter of the centroid of the beam on the target. The measurement data take into account the beam jitter respect to the RF phase noise inside the deflector and are shown in figure 8(a). The resulting time jitter is $\approx 90 f s_{RMS}$. The second method is to observe the jitter of the beam centroid on the time axis projected in the EOS camera. Since the system uses a replica of the PC laser pulse to sample the longitudinal electron beam shape, we measure the relative time jitter between the bunch and the laser arrival time at the EOS station. We observed $\approx 80 f s_{RMS}$ and the acquired data are shown in figure 8(b).

4 Control system upgrade

To include the new locking features in the control system, we upgraded the applications running on both the front-end and the control room CPUs. A full overview of the SPARC RF low level control system is reported in [6].

A new sub-class called LCK (LoCK) has been added in the RFS SPARC control system class. It includes all the parameters necessary to control the electronic board described in section 2.2. Basically it controls the electronic devices described in the lower dashed square part of figure 7.

4.1 RFS software class upgrade

In this paragraph we will go through the description of the specific items that constitute the static and dynamic elements of the LCK sub-class. The reader can refer to figure 9 that shows the cited LCK elements.

• Static element

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Fit dPhi_dV a0 0	PHS AO Channel D	PZT AO task	Amplitudes
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Figure 9: LCK sub-class static and dynamic elements

- **LCKmotorSTA:** static field about the stepper motor for the laser cavity mirror coarse positioning
 - **COM number:** the number of the serial port used to communicate with the motor driver
 - **Motor axis:** the number of the motor axis to be controlled (the motor has only one axis)
 - **Init position:** the position where the motor should placed after homing to obtain a suitable cavity length
- LCKcardsSta: static fields about the ADC/DAC/DIO PCI cards
 - **DIO card ID:** digital I/O card number
 - **HF lock DIO port/line:** digital I/O channel to activate the harmonic PLL MIRA vs RF (@2856MHz)
 - LF gate DIO port/line: digital I/O channel to activate the gate using the fundamental PLL MIRA vs FLAME (@79 + 1/3MHz)
 - **Reference DEM err/corr:** number of DEM sub-class elements (waveforms) linked to the LCK element for both error and correction signals display and analysis. It is related to the harmonic loop.

- **Reference DEM err/corr:** number of DEM sub-class element (waveform) linked to the LCK element related to the fundamental loop.
- **LCKpztSTA:** static fields to control the piezoelectric motor for cavity mirror fine positioning

PZT AO card ID/channel: DAC card/channel that control the piezo driver

LCKphsSTA : static fields to control the LF phase shifter for choosing the "RF bucket" within the HF loop is acting

PHS AO card ID/Channel: DAC card/channel that controls the phase shifter

Fit dPhi_dVa*: fit parameters for the derivative of phase vs volts phase shifter characteristics. It is used to jump directly from an RF bucket to the next (or previous)

• Dynamic element

Lock Status: ON/OFF status of the HF lock

- **HF Track Status:** ON/OFF status of the HF tracking (follows slow drifts with stepper motor)
- HF Track Treshold: piezo voltage threshold value to activate tracking system
- LF gate Status: ON/OFF status of the LF lock
- **LF Track Status:** ON/OFF status of the LF tracking (follows slow drifts with LF phase shifter)
- **LF Track Threshold:** quadrature mixer signal (Q) voltage threshold value to activate tracking system
- **Unlock Threshold:** Piezo voltage value (close to the maximum) to automatically deactivate the PLL
- **Reset TSH AVG:** When PLL is turned ON this flag is used to reset the signals average used to compare with the threshold
- **LCKmotorDyn:** dynamic fields to control the stepper motor inside the optical cavity
 - **Target position:** position to be reached by the motor after receiving a move command
 - **Current position:** display the position of the motor wheter it is moving or not

Controller error: error status of the motor controller

- LCKpztDyn: dynamic fields to control the piezoelectric motor
 - **PZT AO task:** the LabVIEWTM analog output task reference relative to the piezoelectric control
 - PZT AO value: current value assigned to the analog output
- LCKphsDyn: dynamic fields to control the LF phase shifter
 - **PHS AO task:** the LabVIEWTM analog output task reference relative to the LF phase shifter control
 - PHS AO value: current value assigned to the analog output
- LCKcardsDyn: dynamic fields about the ADC/DAC/DIO PCI cards
 - **lock DO task:** the LabVIEWTM digital output task reference to turn ON/OFF the HF feedback
 - **gate DO task:** the LabVIEWTM digital output task reference to turn ON/OFF the LF gate
 - **DC values:** array to store the DC offset of the signals acquired by the ADC card
 - **Amplitudes:** array to store the amplitude (peak value the oscillating waveform) acquired by the ADC card
 - **Frequencies:** array to store the main frequency component of the signals acquired by the ADC card

4.2 Control room GUI application

To control the new devices and achieve the best performance by the harware upgrade, the control room user can use a new dedicated GUI, that can be loaded from the RF main control panel by clicking the "MIRA LOCK" button. The window shown in figure 10 will open up. We will briefly explain the scope of the various sub-panels identified in the figure by different colors.

• Red square

- **PLL ON/OFF:** this is the most used button and it is used to turn ON/OFF the HF PLL (i.e. locking the MIRA to the RF external reference)
- **TRACK ON/OFF:** this button is to turn ON/OFF the tracking feature. When it is ON the stepper motor moves to compensate slow drifts in the length of the



Figure 10: The control room GUI for controlling the new SPARC_LAB locking features

optical cavity to allow the piezo-motor to work in the center of its characteristics (zero DC offset in the waveform). Can be turned ON only if the PLL status is ON. If the machine is running in single laser configuration (only the photo-cathode laser), the operator needs to set only these first two items.

- **2 lasers ON/OFF:** this should be used when the FLAME and the PC laser are both switched ON and the operator wants them to be overlapped in time in one of the SPARC_LAB interaction regions.
- **LF TRACK ON/OFF:** this allows to turn ON/OFF the LF tracking function that acts on the LF phase shifter and preserve the LF gate to change the RF bucket within the MIRA is locked.
- Blue square: This parameter set should be used in 2 laser configuration mode (see section 2.2). The ±1 RF period buttons are used to jump from one RF bucket to another, thus to move in time the PC laser pulse relative to the FLAME pulse in steps of ≈ 360ps.

- Green square: The control located in this area is used to manually move the piezoelectric motor to a fixed position, different from the center of its characteristics. Actually the PZT control value (±3V max. range) is the voltage that the DAC card gives as output towards the piezo-motor driver. This control can set the piezo voltage only if the HF loop is turned OFF.
- **Purple square:** The plots shown in this area reports the waveforms acquired by the ADC card
 - **Upper graph:** here the operator can observe the two waveforms relative to the HF loop. More precisely the error signal and the correction signal are reported. They are respectively measured before and after the loop error amplifier.
 - **Lower graph:** this graph reports the quadrature signal from the phase comparison of the MIRA and FLAME oscillators. This gives indications on the working point of the LF gating system.
- **Orange square:** This part shows the results of the analysis on the waveforms performed by the front-end CPU and used to automatically track slow drifts and to determine if the loop is performing as expected. Also there is a sort of "interlock" functionality that switch the loop OFF if the correction signal average is outside the *Unlock Threshold* set in the LCK dynamic variable.
- Yellow square: Here are reported the controls and indicators concerning the stepper actuator and motor driver to coarse correct the length of the MIRA optical cavity. The operator can move the motor by single step (or fraction) or by setting a desired target absolute position (relative to the last homing). Also a table to read the controller error codes and status is available.

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References

[1] M. Ferrario et al., Proceedings of IPAC2013, Shanghai, China, TUOCB102

- [2] R. Boni et al., in Proceedings of LINAC2012, Tel-Aviv, Israel, MOPLB09
- [3] M. Bellaveglia, A. Gallo, C. Vicario, in EUROFEL-Report-2006-DS3-027
- [4] M. Bellaveglia, et al., in Proceedings of DIPAC09, TUPD30
- [5] R. Pompili, in PhD Thesis 2013, www.infn.it/thesis/thesis_dettaglio.php?tid8140
- [6] M. Bellaveglia, Tech. note SPARC-CS-12/008, www.lnf.infn.it/acceleratori/sparc/TECHNOTES/CS/SPARC_CS_12_008.pdf