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SPARC Timing System: Design and User Manual

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ABSTRACT

Goal of SPARC Timing System is to produce clocks and low frequency triggers, locked to the SPARC main oscillators to operate LINAC and diagnostics as well as timed experiments like Seeding.

This report gives a description of the SPARC Timing System. The document starts to explain the design general approach, describing the main Timing building blocks, and then it includes a small user manual. Both chapters try to answer to the frequent asked questions coming from the SPARC operators.

1. Introduction

Goal of this note is to give a general description of the Timing System implemented for the Project SPARC (Sorgente Pulsata e Amplificata di Radiazione Coerente) [1], the Free Electron Laser built at the Laboratori Nazionali di Frascati after approval in March 2002.
The SPARC Timing System generates pulses and clocks to be used by diagnostics, radio-frequency and laser systems, both for photo-injection and seeding. At the end of the year 2010, the system has been updated by designing a new module to generate 1 kHz frequency clock locked to the main RF frequency. As a consequence, the Timing System general interconnections have been modified and this document wants to describe and to clarify the new system setup.
The SPARC Timing System must not be confused with the SPARC Synchronization System developed by A.Gallo and M.Bellaveglia with different goal and design.

2. General Description

The SPARC Timing System is composed by several building blocks that are shortly described in the following paragraphs.

First of all a COTS (commercial, off-the-shelf) device, the DG535 digital delay generator by SRS (Stanford Research System), is used as PLL and fanout to generate triggers locked to the "line" (the main power supply). This unit is labeled DDGSP002 (with GPIB address 14). The 50 Hz signal, coming from ENEL electricity distribution network, has typically a peak-to-peak jitter of ~ 0.1/1000 of the period. In other words, from hit to hit, every new pulse can have up to 2 μs displacement respect to the expected time.
It is important to be locked to the power supply frequency for two reasons:
a) to have a beam synchronous with the magnet power supply ripples to limit instabilities and other undesired effects on the beam due to time-varying magnet performance (even if very small);
b) to have better performance for all the electromagnetic diagnostics that in general can suffer 50 Hz (and its harmonics) noise and ripples limiting device dynamic range and precision.
The DDGSP002 unit is programmed to mask 4 every 5 pulses and, in this way, it is possible to reduce the clock output from 50 to 10 Hz. This setup can be also modified remotely to have a different gun rates, from single shot up to 50 pulses per second. Note that this feature has never been used up to now.

The "Fast Timing" is the main module of the system. This board has been designed in 2005 at LNF [2] to lock in phase the main radio frequency clock (2856 MHz), the Laser Oscillator frequency (79.333 MHz), as well as other needed low frequencies as 1kHz and 10Hz, from the main power supply (i.e. from ENEL electricity distribution network).
The "Fast Timing" is based on ECL components (mainly digital programmable dividers) and fits in a NIM crates. It has three input signals, placed in the real panel.
From top to bottom they are:
in1) RF: a clock at 2856 MHz, coming directly from the master oscillator. This signal is coupled in AC with a level of 7-10 dBm. In a different, alternative setup, this signal could come downstream from the radiofrequency system after the main phase shifters. In DAFNE, the LNF e+/e- collider, there are parts of the timing system [3], [4] that are implemented in this way.
in2) LINE IN: a 10Hz clock locked with power supply ripples from DDGSP002. The input electrical level is ECL single ended.

in3) 1kHz IN: in the 2011 updated setup, this frequency comes, through a level adaptor, from the "3 Stages Divider" module, that is part of the SPARC Timing and it is described below. Note that in the past this frequency was generated from the laser system, but it was uncorrelated to the other clocks. The input electrical level is ECL single ended.

The Fast Timing module has five outputs, placed in the front panel, all using SMA connectors. From top to bottom, they are:
out1) RF/36: clock at 79.333 MHz generated by digitally dividing the RF clock by 36. The electrical level is in AC with a ~6 dBm swing if high impedance terminated. The nominal rms jitter with reference to RF input is ~1.5 ps.
out2) RF/36/: as the previous signal but inverted.
out3) RF/4: clock at 714 MHz generated by digitally dividing the RF clock by 4. The electrical level is coupled in AC with a ~6 dBm swing if high impedance terminated. The nominal rms jitter (with reference to RF input) is 1 ps.
out4) RF/4/: as the previous signal but inverted.
out5) GUN_Enable: a 10Hz trigger, NIM level, synchronized with RF, RF/4, 1 kHz and line (i.e. power supply ripples). This signal, being synchronized with power supply 50 Hz as well as the other faster frequencies, of course cannot be simply 1 kHz divided by 100 but it will have a period varying in the range 100 ms +/- 2μs from shot to shot. The GUN_Enable nominal rms jitter with reference to RF input is ~ 3 ps.

The "3 Stages Divider" (SPC-002) module [5] has been designed at LNF in 2010 and has the function to generate output frequencies by digitally dividing the input clock. It is a NIM module allocated in the same crate of the Fast Timing.
The “RF IN” input is connected to the RF/36 clock generated from the Fast Timing board. By implementing 3-stages 8-bit digital divider that can be manually programmed by setting three 8-bit dip-switches, it is possible to produce 1 kHz output clock synchronized with the input signal.
The “OUT F_1”, “OUT F_2”, “OUT S_1”, “OUT S_2” outputs are TTL level signals and the nominal rms jitter (respect to the input) is ~10 ps. One of the output is send to the Fast Timing through another DG535 (labeled DDGSP010, with GPIB address 10) that converts the electrical levels from TTL to ECL and that is also used to distribute signals with programmable delays and electrical levels, as needed for the Seeding experiment.
The GUN_Enable signal, that is the 10 Hz trigger to be send to all the apparatus, like klystron modulators, diagnostics, controls and two laser systems (photo-cathode and seeding) needs to be distributed with different and anticipated phases (i.e. pre-triggers) even if they are all locked to the original pulse coming from the Fast Timing module. This goal is implemented by using two (or eventually more) DG535 digital delay units, labeled DDGSP001 (with GPIB address 15) and DDGSP004 (with GPIB address 11).

To evaluate DG535 [6] performance, the rms jitter versus time delay is plotted in fig. 1 (from the user manual [7]): considering only delay values < 1 ms, the rms jitter is < 60 ps, while the resolution is 5 ps for each output channel.
Recently, a new version of the digital delay unit has become available from same company. It is the DG645 [8] that has reduced output jitter to < 25 ps. This device, if necessary, could be easily implemented to replace the DDGSP001 and DDGSP004 units with a (relatively) modest cost.

Few words about distribution: in the Timing System, the clock and trigger distribution is done by using electrical coaxial cables, type RS-223 (double ground shielding) or Andrew Heliax

type FSJ4-50B, both at 50 Ohm impedance. The coaxial cable distribution is compatible with the system jitter range, given that the SPARC hall length is < 40 m. However, generally speaking, to have stable behavior skew for different length cables, the SPARC room temperature should be reasonably controlled, as it is done for the laser room temperatures.

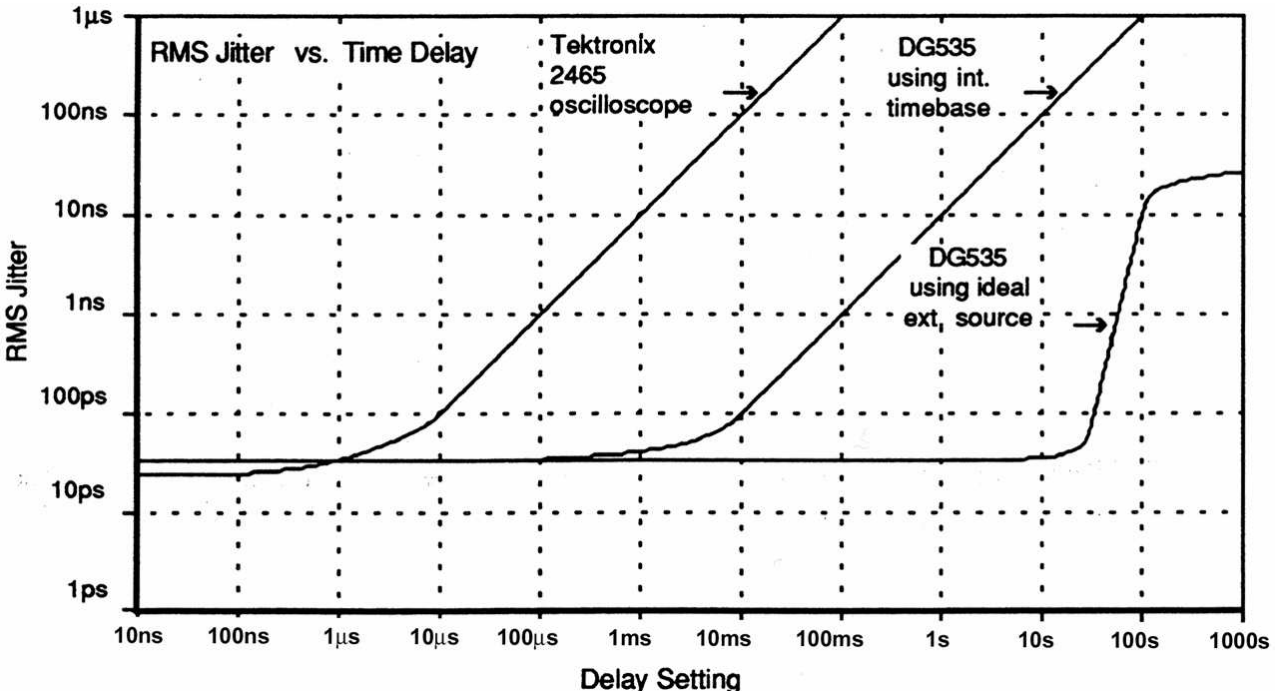

Fig.1 - DG535 rms jitter versus delay setting

3. User Manual

First of all, the DDGSP002 output is programmed with a 95 ms delay to output 10 Hz pulses with 1 ms length and locked to the power supply ripple. The frequency can be modified (also remotely) to have different gun rates, from single shot to 50 pulses per second.

SPARC operators should set very carefully delays in the GUN_Enable distribution chain considering that delay values > 1 ms will produce an increase of the jitters for the devices connected to digital delays DDGSP001 and DDGSP004. For example a 100 ms delay will increase the jitter from 60 ps to 1 ns as it is shown in Fig.1. The logic to program the delays should be that the device asking for more anticipated triggers should be put at the minimum delay value while devices that don't need large anticipations should be set at bigger delay values. Very large delay values (> 1 ms) should be managed by separate digital delay chains connected separately to avoid increasing the jitter in the main distribution chain.

To evaluate correctly the Timing System performance is necessary to make a comparison with the synchronization unit included in the laser.
During February 2011, jitter measurements have been carried on the SDG (Synchronization and Delay Generator for Pockels Cells) unit by Coherent, Inc., provider of the laser system. The SDG data sheet [9] declares 250 ps delay step size and < 250 ps timing jitter. All the tests done in the LNF laboratory have shown that the jitter introduced from the DG535 unit, if setup delay values are < 1ms, is smaller than the SDG jitter.
Furthermore the tests have shown that the SDG unit, that has two clock inputs (10 Hz and

79.333 MHz), can be used in two ways, chosen by setting the external switch put on the device :
a) synchronizing (or re-synchronizing) 10 Hz input with the 79.333 MHz clock by using the internal TTL flip-flop;
b) avoiding to synchronize (internally to the SDG) the 10 Hz input signal.
The case a), showing smaller output jitter, has to be carefully checked because laboratory tests indicate that any infraction to the setup/hold time in the internal flip-flop produces unpredictable (i.e. not synchronized) output results. Practically this means that in the a) setup, the physical skew between the two input signals must be always monitored and, if necessary, changed within 12.6 ns period by an analog trombone delay or similar unit, possibly with remote control.
The b) setup, if the 10 Hz input is already sufficiently synchronized with the 79.333 MHz, does not need any other correction or skew management. In this case the SDG unit basically works as a fanout module.

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