Neutron Induced Single Event Upset Dependence on Bias Voltage for CMOS SRAM With BPSG

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Abstract—We have measured the Single Event Upset (SEU) probability of a static random access memory (SRAM) under neutron irradiation as a function of the memory 6 T cell bias voltage supply. In these memories the presence of a BoronPhosphorSilicateGlass layer induces the memory state upset as a consequence of ¹⁰B neutron capture reactions. The Single Event Upset (SEU) probability versus voltage bias curve was evaluated in the neutron radiation field produced by various electron linacs and in a thermal neutron beam of a nuclear reactor. For these different spectra with neutron energies below 5 MeV the upset behavior curve exhibits a universal shape independent of the installation. The circuit level together with the physical level ion energy deposition simulations allow to reproduce the measured curve. The experimental curve shows a characteristic shape that depends on the statistical distribution of ionization on the charge collecting volume, and consequently on the geometry details of the SRAM and alpha and lithium transport. When the SEU effects in such components are considered for thermal neutron fluence estimation, the present work allows the selection of optimal bias voltage.

Index Terms—Borophosphorosilicate glass (BPSG), neutron, single event upset (SEU), static random access memories (SRAMs).

I. INTRODUCTION

S INGLE EVENT UPSETS (SEU) in digital devices are produced by the ionization charge released from the interaction in silicon of particles like heavy ions, alpha particles, recoil nuclei or nuclear fragments from neutron interactions. The discovery of these effects came originally from electronic systems exposed to space radiation [1], [2]. Static random access memories (SRAMs) change the logical level of their cells when are exposed to neutrons, although their sensitivity depends enormously on the cell design, chip layout and materials [3]. In a seminal work by R. Baumann, it was first identified that the boron fission due to its presence in some of the chip layers

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can be a dominant process for neutron induced soft errors in digital devices [4]. Borophosphorosilicate glass (BPSG) layer, commonly used in complementary metal oxide semiconductor (CMOS) SRAM-memory until the beginning of 21st century, triggered the production of a significant number of Li nuclei and alpha particles when exposed to slow neutrons. These highly ionizing Li and He ions (with maximum range in silicon of 2.8 μ m and 6.4 μ m respectively) produce significant ionization charge in a small volume that is able to induce a current pulse in memory cells changing their logical state when a threshold current is exceeded. Starting, in our case, from all cells in a given logic level and after exposure to neutron fluence, the SEU produced are counted as the number of logic level transitions in the full array. The number of SEU is proportional to the neutron fluence and this number is also a function of the memory component bias voltage because the upset threshold current and the collected charge distribution depend on the voltage supplied to the memory cell transistors. Although this behaviour could be considered a detriment of the component, some of the authors have proposed and used this kind of effect to evaluate the slow neutron fluence in mixed radiation fields of radiotherapy rooms [5], [6]. The SRAM used in this work represents an old generation of 0.4 μm bulk CMOS technology that proved extremely reliable and simple to operate in mixed gamma/neutron radiation fields and provided an active instrument able to make measurements in the pulsed neutron radiation field of a electron linac [6], [7]. This work is focused in the characterization of the neutron SEU sensitivity dependence with the SRAM bias voltage used for the radiotherapy application. This dependence is crucial for the optimal use of this device to estimate radiotherapy patient exposure to neutrons and its uncertainty. There have been different efforts to use new semiconductors designs for neutron detection such as coated thin film diodes [8] or 3D microstructured/perforated detectors [9]. Although intrinsic efficiency in these devices is much higher than in the SRAM array, the analog signal has to be properly processed in order to work in pulsed mixed photon-neutron radiation fields. Thus, the solution of the SRAM system provided a very reliable and simple baseline detector for thermal neutron detection being intrinsically insensitive to photons.

II. MATERIALS AND METHODS

Memory Boards: For the evaluation of the upset of memory states, we have developed a dedicated board (N-MON) with 128 SRAM memories (Samsung K6T4008) of 512 KiB size with 8 bit words. This board is accessed through an embedded microcontroller that has a slow RS232 interface control to communicate with the remote computer user application, as shown

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Fig. 1. Board used for the measurements and block description.



Fig. 2. Neutron lethargy for a medical linac working at 15 MV. Fluence is normalized to 1 Gy photon dose.

in Fig. 1. The system is configured to perform memory reset and SEU counting from single serial interface commands. Additionally, SEU scoring can be performed by memory sectors or globally for the whole board. To bias the memories, a dedicated programmable power supply was integrated with the data adquisition program in order to provide the transition from standby to nominal (5 V) voltages used in irradiation and read/write modes respectively. This board is a new version of a previous system called NEUTOR [10]. The content of the whole memory array was set to a low logic state and put in standby mode (low bias) before neutron irradiation. After irradiation, the array was biased at nominal voltage, read and the number of high logical bits was counted.

Irradiation Facilities: Two kind of irradiations were performed: exposing the boards to the neutron fluence inside a radiotherapy room and to the thermal neutron beam from a nuclear reactor. Inside the radiotherapy linac rooms, the photonuclear reactions triggered by high-energy photons in the accelerator gantry produce evaporation neutrons with an energy around 1 MeV. Neutron transport inside the room produces thermalization in a few milliseconds, mainly through scattering with the concrete walls. Thus, the neutron spectrum inside the room has a characteristic primary neutron peak around 1 MeV and a large fluence of slow scattered neutrons with energies below 1 eV [11], [12]. The three facilities involved in this work were located at three hospitals in Seville, Rome and Santiago de Compostela. In the radiotherapy rooms the boards were placed in the gantry axis plane at a distance of approximately 2.5 m from isocenter. Under these irradiation conditions, the average total neutron fluence rate is around 8×10^4 n cm⁻² s⁻¹ (with variations between installations due to the room size and linac model). A typical neutron energy spectrum in a medical facility can be seen in Fig. 2.

For the thermal beam irradiation, the board was placed in the external port of the Portuguese research nuclear reactor of Instituto Superior Técnico (Lisbon) working at around 1 MW [13]. The thermal neutron fluence rate was approximately $1.4 \times 10^5 \text{ n cm}^{-2} \text{ s}^{-1}$. The irradiation runs were performed with continuous beam in 60 s intervals.

SEU Modelling: Three dimensional ion transport and ionization calculations were performed through *TRIM* simulation from the *SRIM 2013* package [14] to obtain the deposited energy in the silicon collection volume around a transistor node in the cell. Thus, this energy deposition can be translated to a transient current pulse amplitude I_{trans} in the form

$$I_{trans} = \frac{e}{w} E_c \times \frac{1}{\tau_c} = k \times E_c$$
$$k = \frac{e}{w\tau_c}$$

where E_c stands for the energy absorbed through ionization processes around the track within the collection volume, w is the average energy per electron-ion pair in silicon, e is the electron electric charge and τ_c is the effective collection time. From the collision event by event simulation of the ion transport it was obtained a distribution of charge ionization along the track. This ionization cloud will drift according to the electric field present in the silicon substrate. For a given transistor configuration it was assumed that the transient current was due to the charge produced inside an effective collection volume. The average distribution of upset events per unit of neutron fluence in the SRAM can be considered as the number of events over a certain energy threshold depending on the voltage applied

$$N_{SEU}(V) \propto \int\limits_{E_{th}(V)}^{E_{max}} f(E_c) dE_c = \int\limits_{rac{I_{th}(V)}{k}}^{E_{max}} f(E_c) dE_c$$

where $f(E_c)$ is the density function for the energy deposited in the collection volume. Considering the relation between the collected charge and energy, this relationship can be used to relate the number of SEU at a certain voltage V respect to a reference voltage V_0 (in our analysis $V_0 = 2$ V).

$$S(V, V_0) = \frac{N_{SEU}(V)}{N_{SEU}(V_0)} = \frac{\int_{\frac{I_{th}(V)}{k}}^{\frac{E_{max}}{k}} f(E_c) dE_c}{\int_{\frac{I_{th}(V_0)}{k}}^{\frac{E_{max}}{k}} f(E_c) dE_c}$$

The sensitivity function $S(V, V_0)$ represents the relative variation of the SEU cross section as modeled in other previous works [15]. For practical reasons we have normalized the relative variation of this cross section, taking V_0 equal to 2 V in all the data. In the present model, the threshold current was obtained from a *PSPICE* simulation of the six transistor cell that gives the fast current threshold as a function of the bias voltage, thus providing the $I_{th}(V)$ function depicted in Fig. 3.

A Secondary Ion Mass Spectroscopy analysis of the chip gave a detailed elemental content and depth distribution of the chip materials. From that data we built a simulation with a BPSG



Fig. 3. Upset threshold current simulated for the CMOS transistor technology used in this work as a function of bias voltage from circuit simulation level.

layer that covered a two micron depth over the transistor structure. In the TRIM simulation, a random distribution of capture events was generated inside the BPSG layer, with 94% (6%) of events having 1.47 (1.78) MeV and 0.84 (1.01) MeV kinetic energy for helium and lithium respectively [16]. The simulation cell covered 10 μ m \times 10 μ m \times 10 μ m with the collection node in the center of the simulated geometry. A total of 10^5 events were simulated for both helium and lithium ions. The electronic collision absorbed energy scoring was performed considering that the collection volume was an ellipsoid in the silicon layer and afterwards finding the optimal k parameter for the obtained data. The SEU cross section versus bias voltage is very sensitive to the dimensions of the effective collection volume. This high sensitivity was used to discard most of the charge collection geometries performing multiple simulations and selecting a narrow interval for the parameters of the model.

III. RESULTS AND DISCUSSION

The results of the irradiation in the different facilities are summarized in Fig. 4. Although the neutron spectra from the linac facilities and the nuclear reactor neutron beam are quite different, the dominant low-energy boron capture interaction channel provides an almost universal footprint of the memory sensitivity. This can not be extrapolated to neutron beams with energy higher than 5 MeV since there are additional interaction channels that contribute to SEU in that situation [5], [17]. Nevertheless, the data agreement is outstanding since irradiation condition geometries varied from place to place and, in the thermal neutron beam, the board was only partially illuminated. The experimental data exhibit a slope change for a bias voltage around 2.5 V.

Although the component manufacturer recommends a data retention mode voltage over 2 V, we have used bias voltages as low as 1.3 V, verifying through additional measurements that spurious switching of the logical level in the SRAM cells is below 0.5% of the total neutron induced SEU count. On the other hand, the slope of the $S(V, V_0)$ curve around V_0 equal to 2 V normalization point is $-(0.39 \pm 0.02) \text{ V}^{-1}$. Thus, the



Fig. 4. Experimental sensitivity curve for various electron linac facilities and for the IST nuclear reactor thermal beam port. The weighted average of the whole data set is also displayed.

uncertainty in the bias voltage contributes to the uncertainty of the SEU count through this sensitivity coefficient. For example, a 50 mV uncertainty in the voltage supply would imply a 2% relative uncertainty in the SEU total count.

Although there are different approaches for the simulation of the sensitivity of CMOS SRAM at reduced bias voltages, their three key model ingredients are namely: ionization statistics in the sensitive volume, charge collection and transient current generation in the memory cell [18], [19]. In principle, a reduction of the bias voltage could be associated to a decrease in the charge collection volume [15] following the electric field modification. However, our results tend to indicate that a very good agreement between model and data can be achieved keeping that collection volume as constant and considering only the bias effect in the threshold upset current.

In fact, the volume that best reproduced the observed data corresponded to an ellipsoid half with main axis values of 0.7 μ m, 0.5 μ m (transversal) and 5 μ m (depth) in silicon shown in Fig. 6. The chi-square over the number of degrees of freedom corresponding to Fig. 5 data to model comparison is represented in Fig. 7 for different ellipsoid depth with same transversal dimensions, showing an optimal agreement for 5 μ m silicon depth.

The distribution of the energy deposited in the collection volume through electronic collisions is shown in Fig. 8. It is interesting to note that the relative Li contribution to the total energy deposition increases when the energy considered is decreased, reaching almost a 50% at very low energies. The distribution exhibits a cut-off around 400 keV due to the energy loss in the BPSG layer before reaching the silicon collection volume. On the other hand, there is a small plateau below 250 keV that appears to be responsible of the slope change observed in Fig. 4 when bias voltage is close to 2.5 V. The majority of the events produce a very inclined ion track crossing the collection volume and depositing a fraction of the total ion energy as seen in Fig. 9. The balance between the number of events that produce ionization in the collection volume versus the fraction of energy deposited gives rise to the energy distribution of



Fig. 5. Weighted average experimental data together with the model prediction (see text for details).



Fig. 6. Layout of the modelled geometry and the ellipsoid charge collection volume.

Fig. 8. Only a few events with almost vertical tracks are able to reach an energy deposition close to the maximum ion kinetic energy. The authors have considered many other geometries for the charge collection volume (i.e. rectangular, spherical, etc). Fortunately, the comparison of the different models with the data of curve of Fig. 4 discards the vast majority of the other geometries considered. The sensitivity of the model both to the layer geometry and the collection volume is high enough to discard ellipsoids with differences in the main axis higher than 0.3 μ m respect to that shown in this article.

IV. CONCLUSION

We have determined the relative sensitivity variation for SEU in 0.4 μ m technology BPSG layered SRAM memories with the



Fig. 7. Chi square over the number of degrees of freedom from the model and experimental SEU sensitivity curve as a function of ellipsoid collection volume depth in silicon.



Fig. 8. Distribution of the energy deposited in the collection volume both for alpha and Li ions.



Fig. 9. Scatter plot of the deposited energy versus the projected transversal distance of the boron capture event to the center of the transistor node.

standby cell bias voltage. The measured results obtained in dif-

ferent medical electron linac rooms and in a thermal beam from a research nuclear reactor show the same behaviour curve with no significant dependence on the detailed neutron fluence energy distribution. Due to the dominance of the neutron capture reaction cross section at low energies, the kinematics of the nuclear reaction products remains independent of the detailed neutron energy spectrum. This makes the relative SEU cross-section vs SRAM bias voltage essentialy independent of the neutron energy spectrum present in each of the installations considered, while the absolute SEU cross-section would be quite sensitive to this spectral shape. The results have been accurately reproduced using a model of the BPSG layer and silicon layers by propagating the ions produced through ¹⁰B thermal neutron capture in this geometry using the SRIM simulation package. The transient current in the memory cell was considered proportional to the energy deposition in the collection volume through a coefficient k with optimal value 0.13 $\mu A \text{ keV}^{-1}$. The best reproduction of the experimental results are those that consider the charge collecting volume in each transistor node an ellipsold with main axis values of 0.7 μ m, 0.5 μ m (transversal) and 5 μ m (depth) in silicon, Fig. 5. Differences from model and data are within the uncertainties of these values and below 2% in all the measured range from 6 V to 1.3 V, showing an outstanding agreement between both. The detailed collected charge spectrum plays a major role in the relative SEU cross section shape as a function of SRAM voltage. The results show that a coupled circuit to device level description is able to produce an accurate description for the relative cross-section dependence considered in this paper. Nevertheless this methodology would be much less accurate for the absolute SEU sensitivity description.

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