Divisione Acceleratori

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FAST FEEDBACK SYSTEM

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Introduction

In this section, we specify the fast feedback systems for the three oscillation planes (longitudinal, horizontal and vertical) in the ILC electron and positron damping rings (EDR and PDR). The design is based on the following baseline parameters (Table 1).

Parameter	Value
Energy (GeV)	5
Number of bunches (nominal)	2767
Number of particles per bunch	2.0x10 ¹⁰
Number of bunches (max)	5534
Number of particles per bunch	$1.0 \mathrm{x} 10^{10}$
Average current (amps)	0.40
Energy loss per turn (MeV)	8.7
Beam power (MW)	3.5
Bunch current (mA) (nominal)	0.14
RF frequency (MHz)	650
Total RF voltage (MV)	25
Circumference (km)	6.695
h	14516
v _s	.0090
$f_{\rm s}$ (Khz)	4.0
$\alpha_{\rm c}$	4.0e-4
σ_{ℓ} (mm)	6
v_x/v_y	52.28/47.40
τ_{x} (ms)	25.7

Feedback System Specifications

Often, in the past, longitudinal and transverse feedback systems have been implemented in different ways, but now modern technology allows managing bunch-by-bunch correction signals for different oscillation planes with similar or identical blocks. This is true, in particular, for the digital (hardware and software) parts. Today, commercial FPGAs (Field Programmable Gate Array) can easily manage the requirements of the feedback systems in terms of speed and number of bunches.

The bandwidth of the fast feedback system (BWFFB) must be at least f_{RF} (that is 650 MHz). This means that every block of the system must have the capability to manage the full bandwidth except for the power section (amplifiers and kickers), where half bandwidth (BWFFB/2) is sufficient. The main blocks of the systems for each beam line (EDR, PDR) are listed in Table 2. In the Fig. 1 the longitudinal feedback block diagram is shown. The two analog programmable delays are included in the analog front end and the analog back end blocks.

The pickups will be 4-button monitors (two or three for each beam line) with at least full bandwidth (BWFFB) and adequate dynamic range. The analog front ends must be capable of extracting the beam oscillation signals from the monitors in each of the three planes (L, H, V) and giving them to the digital sections with a swing in the range of ~ 0.5 V (typical of many analog-to-digital converters).

Pickup (longitudinal)	picl
Analog front end (longitudinal)	afel
Digital processing unit (longitudinal)	dpul
Analog back end (longitudinal)	abel
Power amplifier (longitudinal)	ampl
Kicker (longitudinal – cavity)	kicl
Pickup (horizontal)	pich
Analog front end (horizontal)	afeh
Digital processing unit (horizontal)	Dpuh
Analog back end (horizontal)	abeh
Power amplifier (horizontal)	amph
Kicker (horizontal - stripline)	kich
Pickup (vertical)	picv
Analog front end (vertical)	afev
Digital processing unit (vertical)	Dpuv
Analog back end (vertical)	abev
Power amplifier (vertical)	ampv
Kicker (vertical – stripline)	kicv

Table 2: Main blocks of the FFB (fast feedback system)

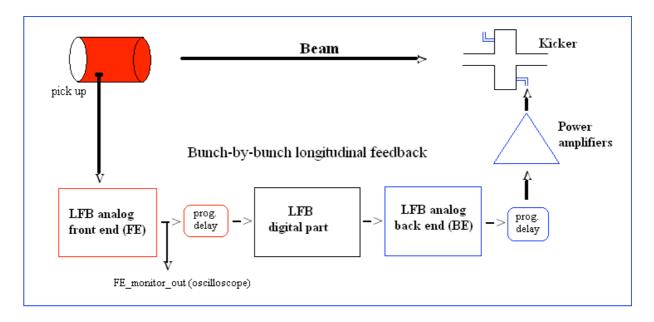


Figure 1: Bunch-by-bunch Longitudinal feedback block diagram.

In the digital blocks (digital processing unit, dpu), it is necessary to minimize the quantization noise and to have an adequate dynamic range. For these reasons, a complete 16-bit signal processing system should be implemented rather than the 8- or 12-bit analog-to-digital converters that are now generally used. The bunch-by-bunch processing unit would ideally be implemented to compute the correction signal for all buckets (including the empty ones) to decouple the feedback behavior from the fill pattern. This means that all feedback systems must have the capability to process, in real time, 14516 input/output channels although the real bunches will only be in 5534 buckets. All the digital blocks must work at full bandwidth, so the sampling frequency is 650 MHz. In the dpu for each channel a real time FIR (finite impulse response) filter (with \ge 50 taps) will be implemented. The correction synchrotron/betatron phase advance will be made by the digital filter so only one pickup will be necessary for each system. Using this approach, the feedback setup will be implemented by the operator using mostly software tools. A down-sampling feature will also be implemented to manage very low oscillation frequencies.

The analog back-end systems must adapt the output correction signals to the power section. Generally the longitudinal kicker (a cavity) will work at a frequency between 800 and 1600 MHz while the transverse kickers (striplines) will operate at baseband (from 10 kHz up to BDFFB/2). Each power section will be formed by four 250-W amplifiers (1 kW total), with the bandwidth required by the kicker. Circulators (for the longitudinal) and power low pass filters (for the two transverse) have to be foreseen to protect the amplifiers from reverse power from the kickers.